Metastable States

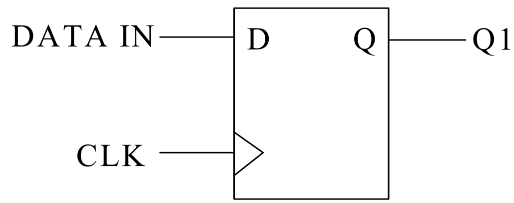
Metastability - Introduction

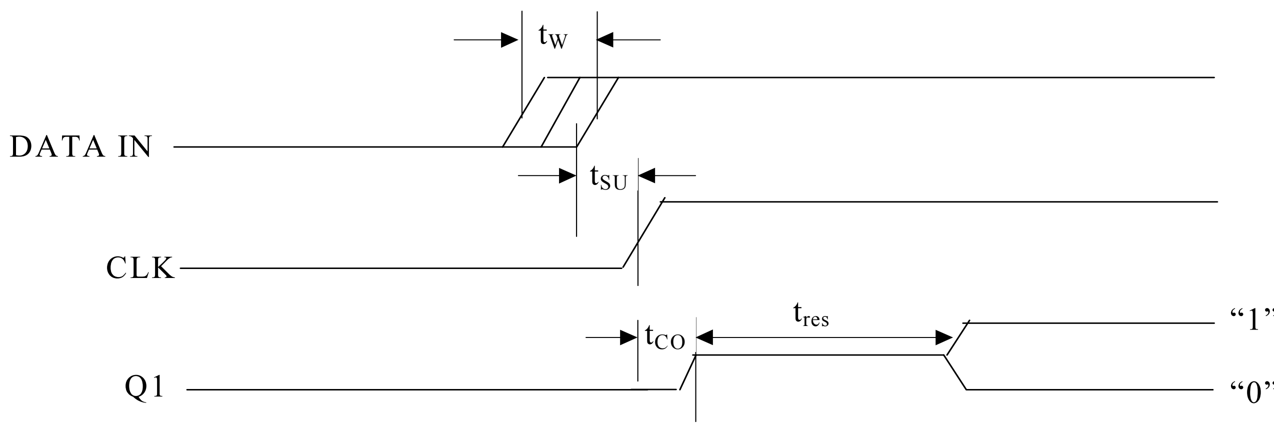
- Can occur if the setup (t_{SU}), hold time (t_H), or clock pulse width (t_{PW}) of a flip-flop is not met.
- A problem for asynchronous systems or events.
- Can be a problem in synchronous systems.
- Three possible symptoms:
  - Increased CLK $\rightarrow$ Q delay.
  - Output a non-logic level
  - Output switching and then returning to its original state.
- Theoretically, the amount of time a device stays in the metastable state may be infinite.
- Many designers are not aware of metastability.

Metastability

- In practical circuits, there is sufficient noise to move the device output of the metastable state and into one of the two legal ones. This time can not be bound. It is statistical.
- Factors that affect a flip-flop's metastable "performance" include the circuit design and the process the device is fabricated on.
- The resolution time is not linear with increased circuit time and the MTBF is an exponential function of the available slack time.

Metastability





t_W = Time window where input transition may cause a metastable condition
t_{SU} = Actual clock setup time for flip-flop
t_{CO} = Actual flip-flop propagation delay
t_{res} = Metastability resolution time

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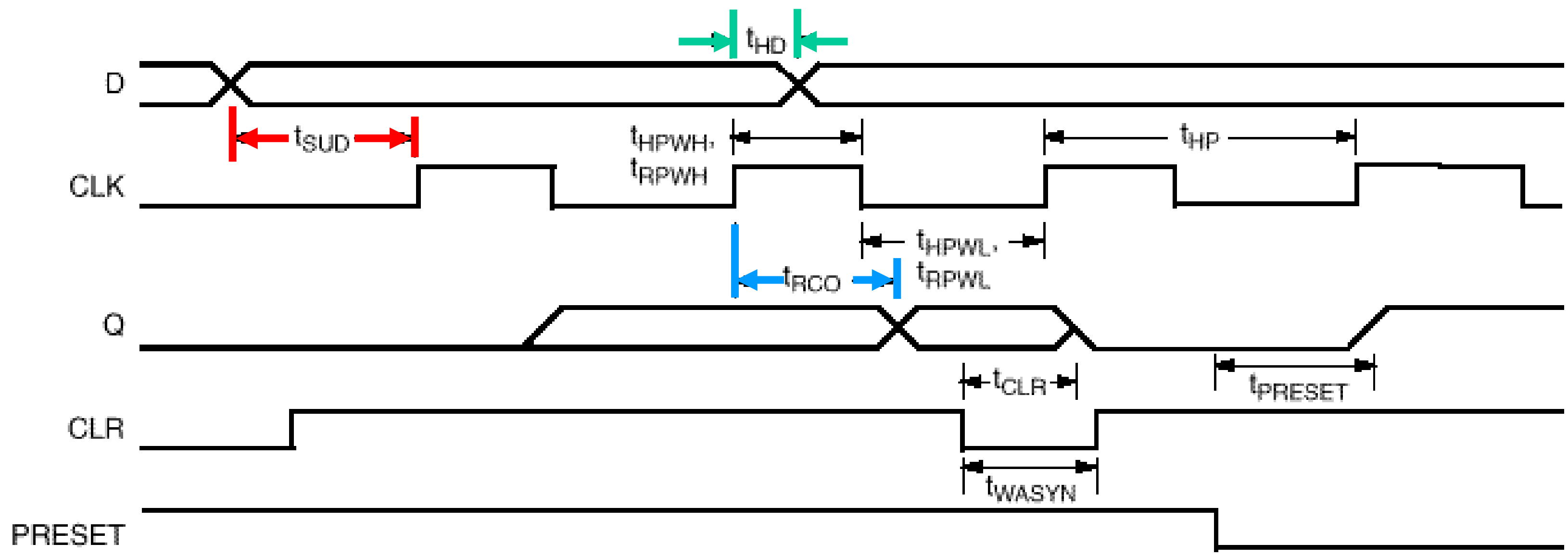
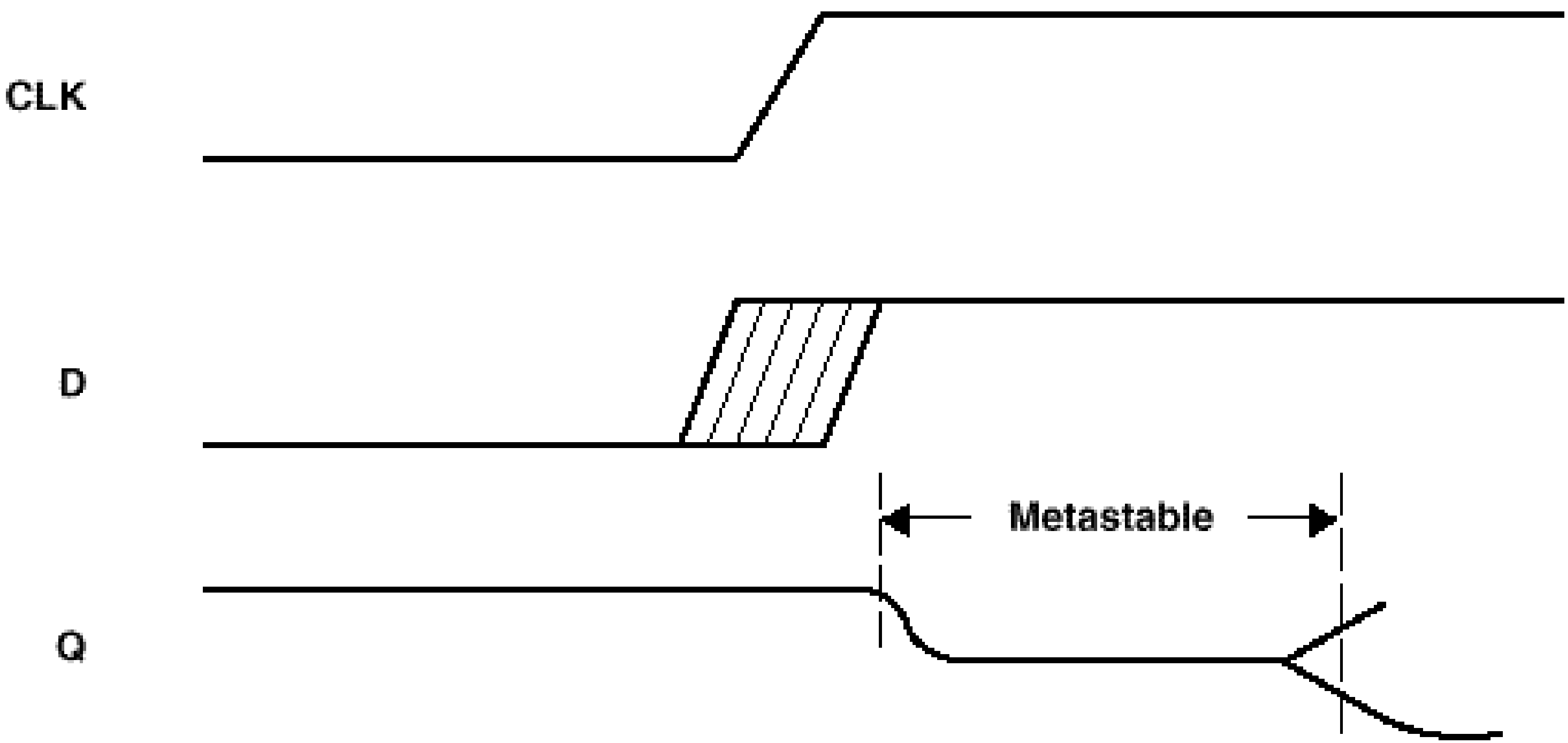
Flip-Flop Timing: RT54SX-S



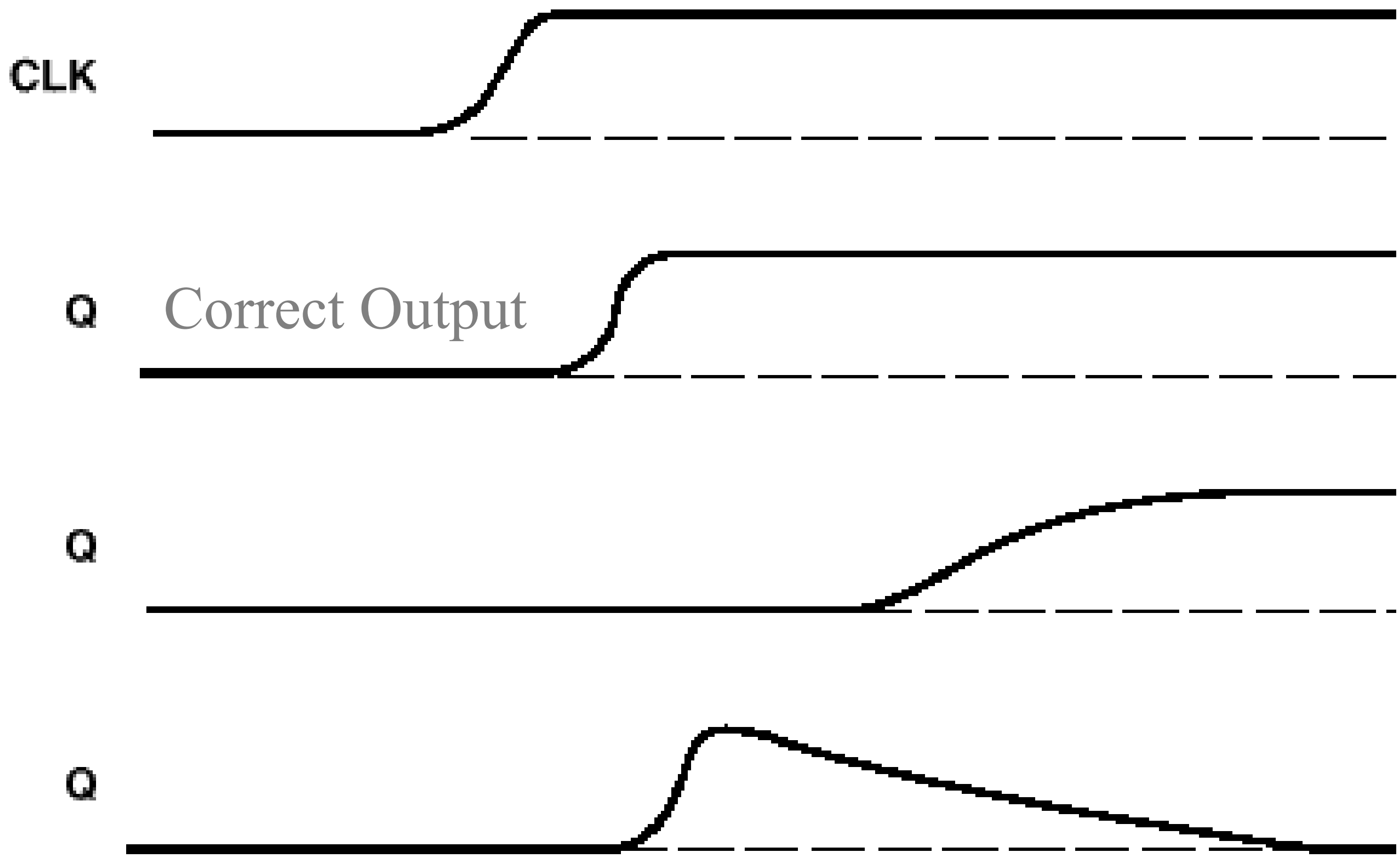
Worst-case Military Conditions, V_{CCA}=2.3, V_{CCI}=3.0V, T_J=125°C
-1 Speed Grade

		Min	Max	Units
t_{RCO}	Sequential Clock-to-Q		1.0	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.6		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.8		ns

Metastable State: Possible Output from a Flip-flop



Metastable State: Possible Outputs from a Flip-flop



Metastability - Calculation

- MTBF = e^{K2*t} / (K1 x F_{CLK} x F_{DATA})

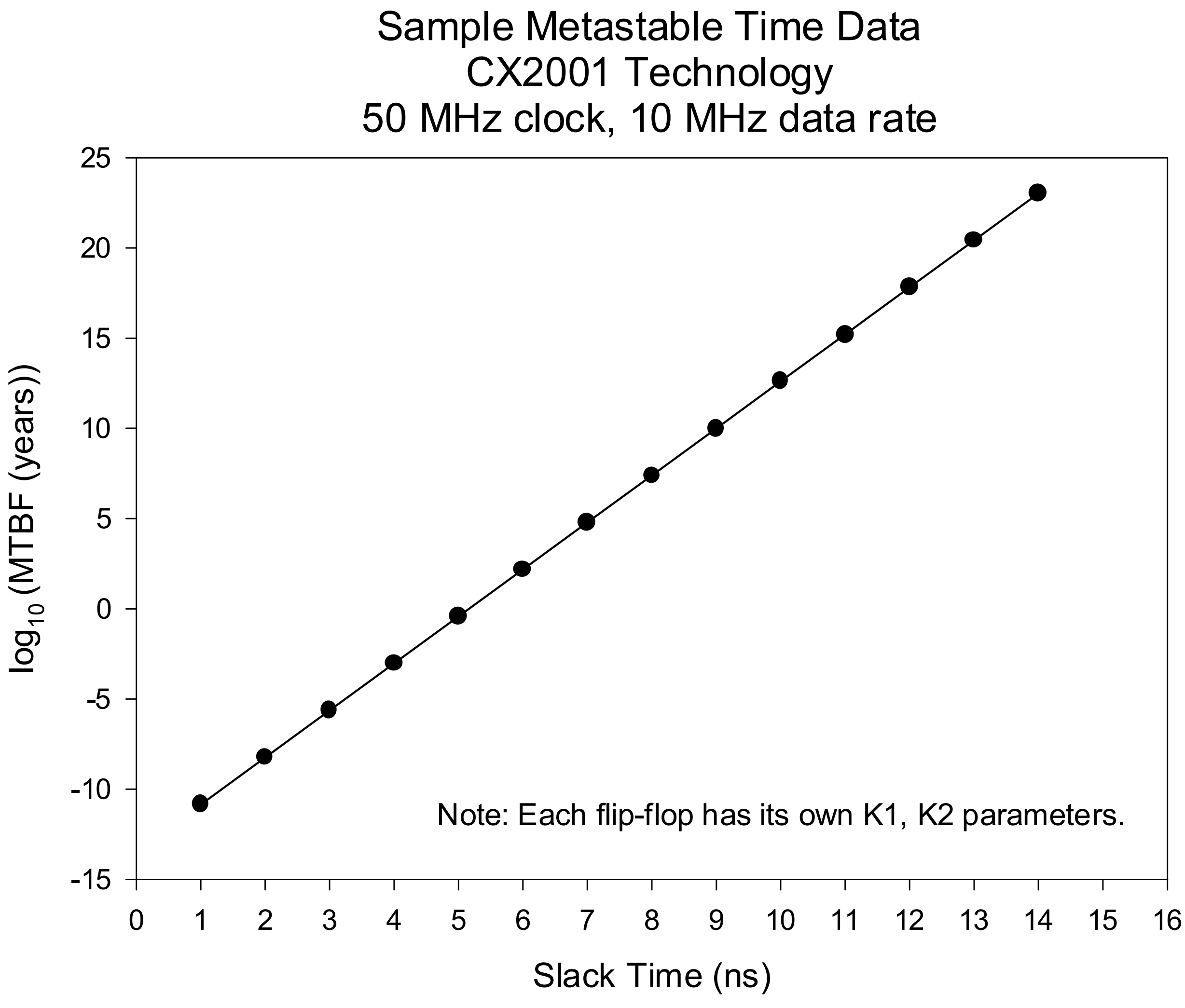
  t is the slack time available for settling

  K1 and K2 are constants that are characteristic of the flip-flop

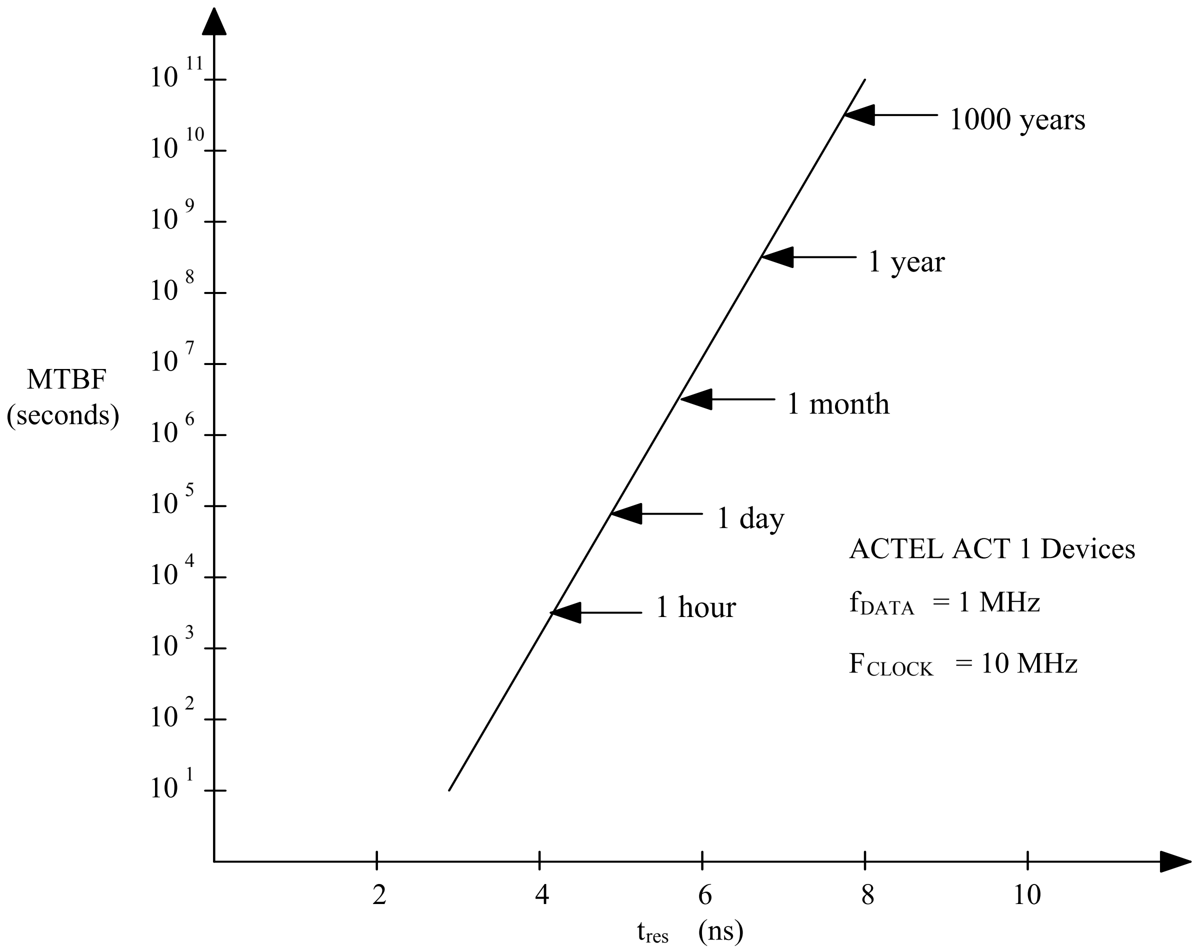
  F_{CLK} and F_{DATA} are the frequency of the synchronizing clock and asynchronous data.

- Software is available to automate the calculations with built-in tables of parameters.
- Not all manufacturers provide data.

Metastability - Sample Data



MTBF versus Metastability Resolution Time



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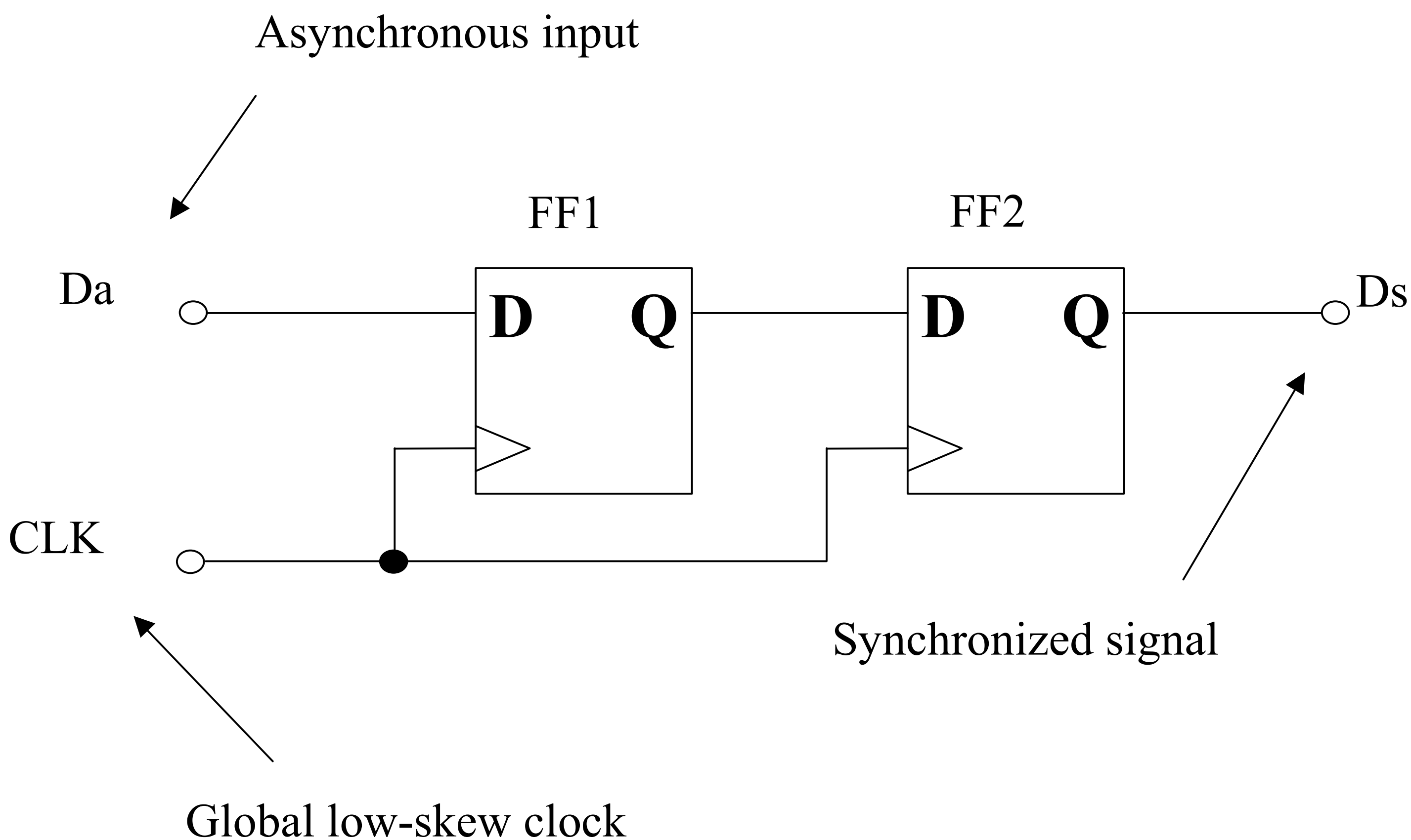
Synchronizer



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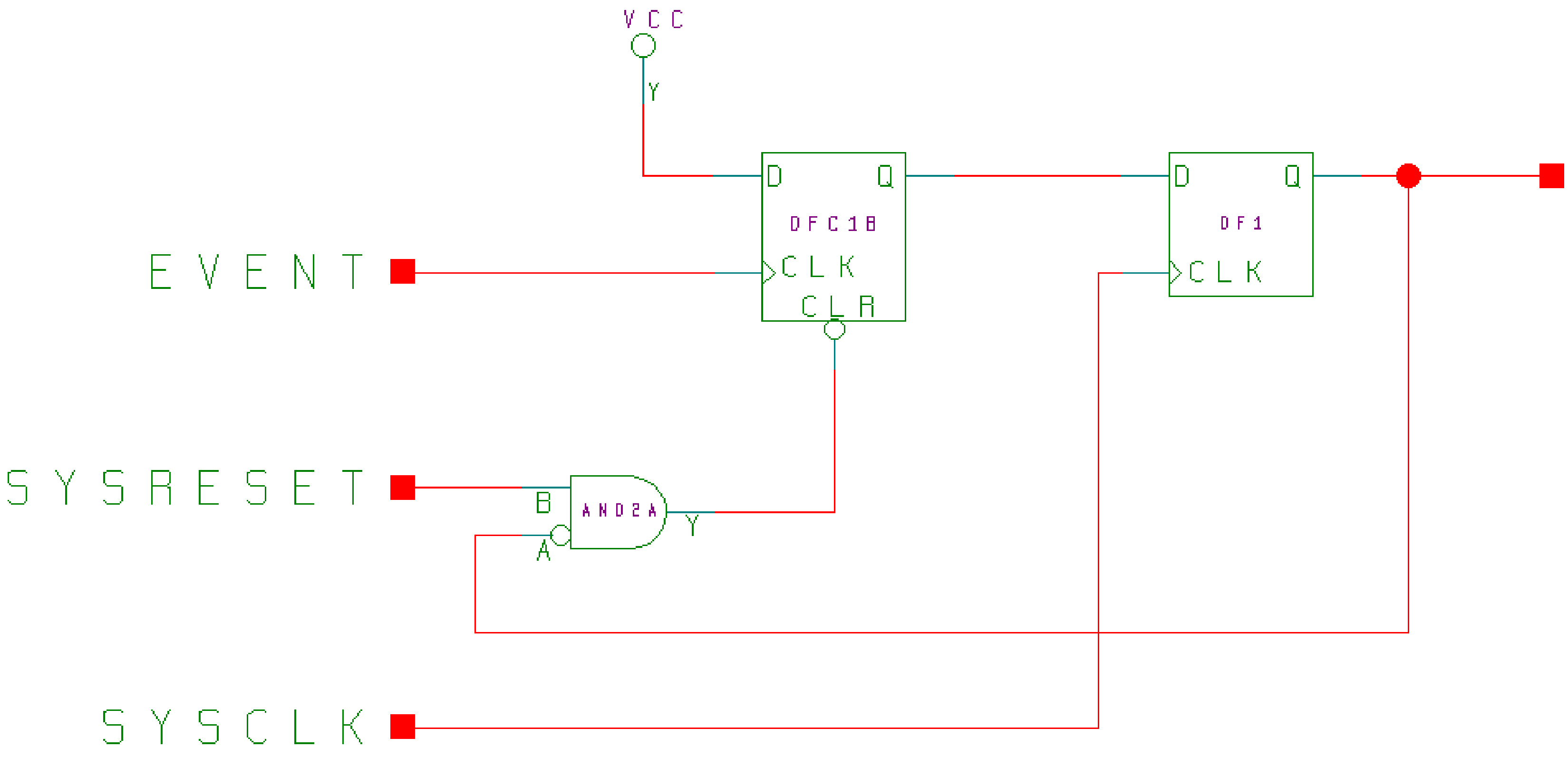
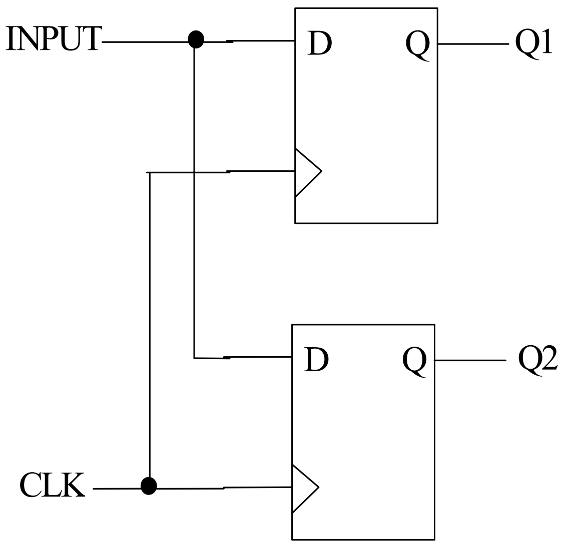
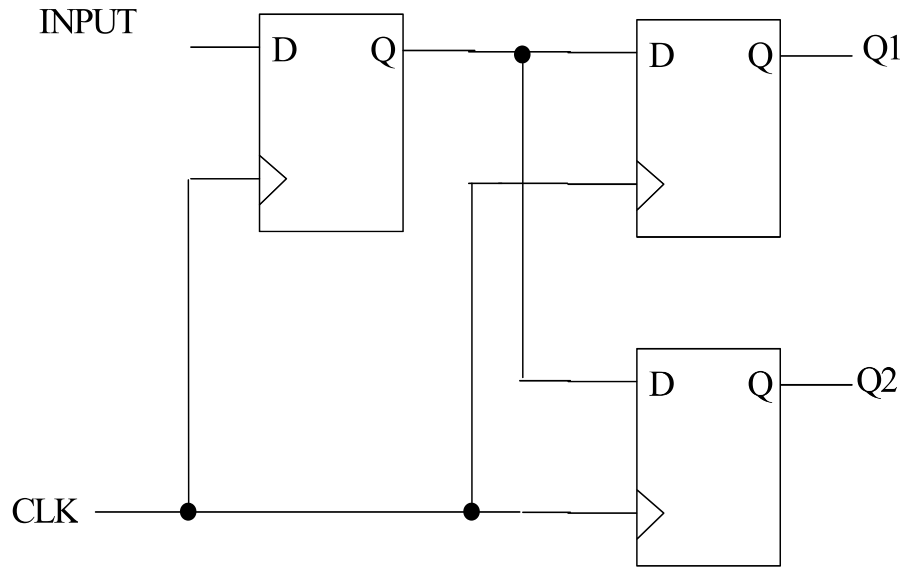
Synchronizer - Bad



Synchronizing an Asynchronous Input



Improperly Synchronized



Properly Synchronized

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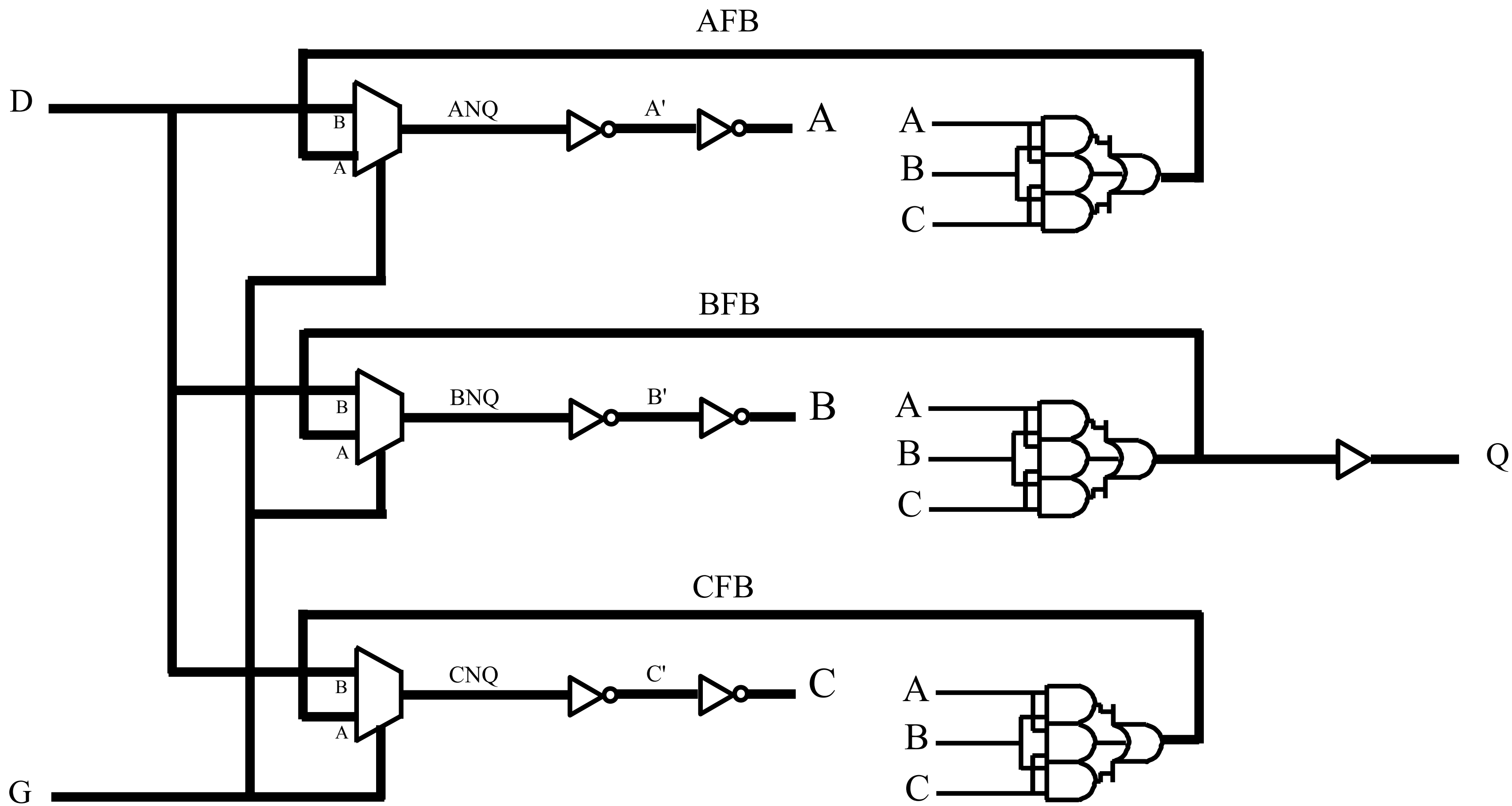
RT54SX-S SEU Hard Flip-Flop

What is its metastable behavior?



Modern CMOS Flip-Flop Example
The Experiment

- CLB flip-flops
- Virtex-II Pro device
  - 130 nmtechnolgy
  - 1.5 Vcc)
- Clock: approximately 350 MHz
- Asynchronous input: approximately 50 MHz
- Measured metastable events per minute

Data from comp.arch.fpga, Peter Alfke, Xilinx Corp.

Modern CMOS Flip-Flop Example

The Test Results

Metastable events/minute for a clock-to-clock delay of:

- 1300 ps: ~ 30,000
- 1400 ps: ~ 2,000
- 1500 ps: ~ 100
- 1600 ps: = 10

Data from comp.arch.fpga, Peter Alfke, Xilinx Corp.

Modern CMOS Flip-Flop Example

The Extrapolation

- Clock = 350 MHz
- Input = 50 MHz
- Allow 1.2 ns for CLK $\rightarrow$ Q + t_{SU} + t_{ROUTE} to the flip-flop in the adjacent CLB, the Mean Time Between Failure (MTBF) will be about 0.1 ms.
- Changing the total delay of 1.2ns to

  - 1.4 ns leads to MTBF = 30 ms
  - 1.6 ns leads to MTBF = 6 sec
  - 1.8 ns leads to MTBF = 20 min
  - 2.0 ns leads to MTBF = 66 hrs
  - 2.2 ns leads to MTBF = 18 months
  - 2.4 ns leads to MTBF = 300 years
  - 2.6 ns leads to MTBF = 60,000 years
  - 2.8 ns leads to MTBF = 12 million years

Extrapolation from comp.arch.fpga, Peter Alfke, Xilinx Corp.

Metastability Numbers

- Many manufacturers do not supply them.
- Many numbers do not come as a guarantee
- Many numbers do not specify the environmental conditions
  - Temperature and voltage can have a large effect
  - Radiation?