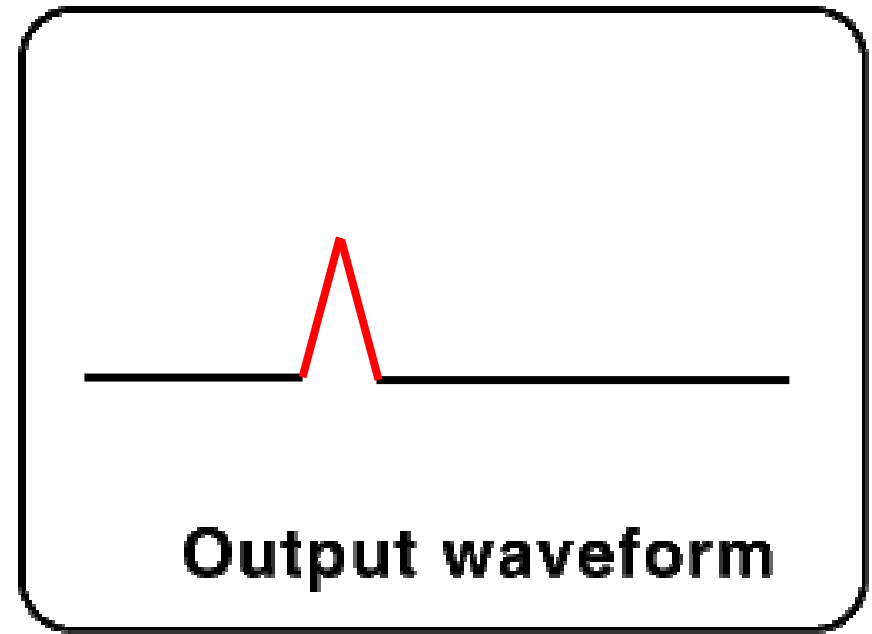
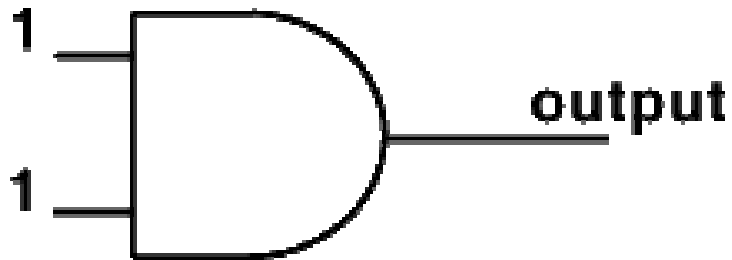


Clock Upset and Finite State Machines

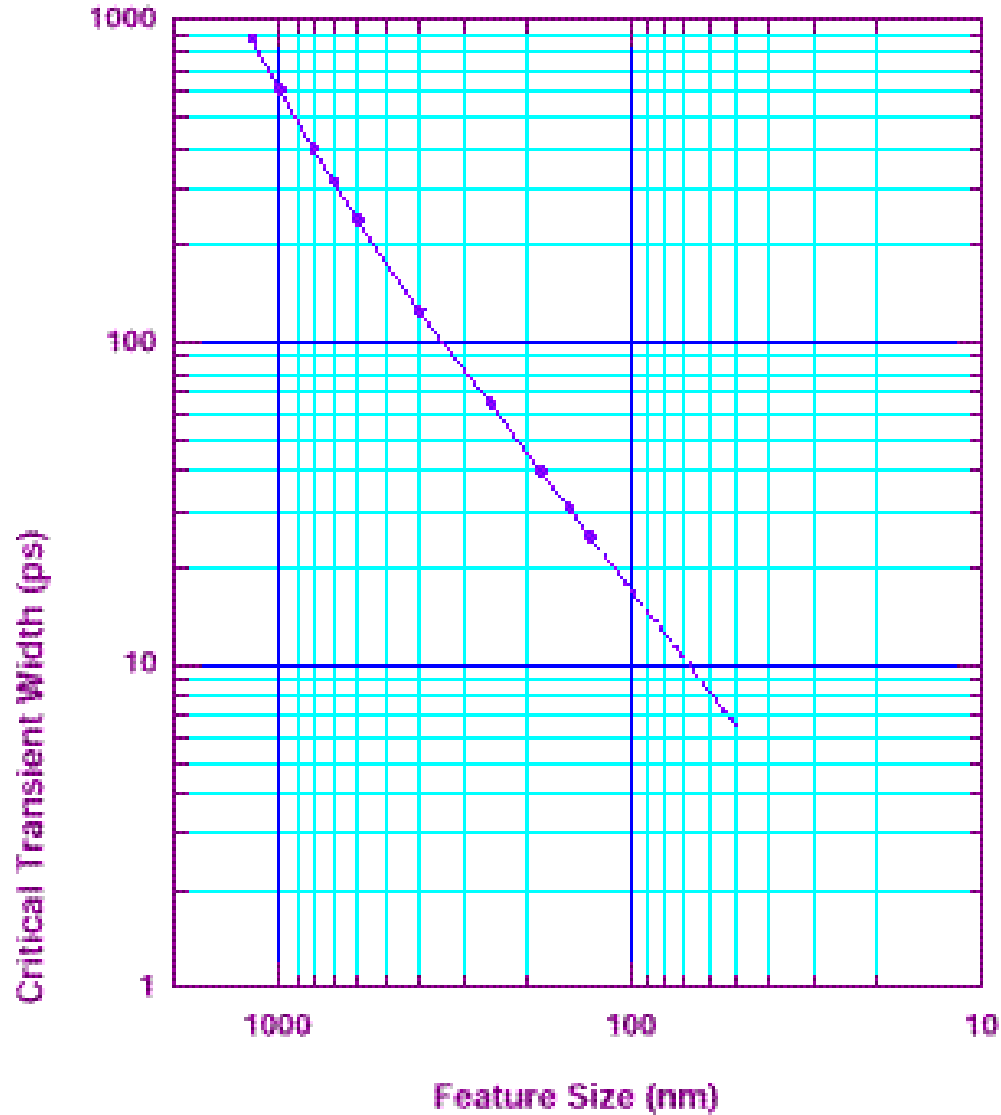
Single Event Transient (SET)



Fraction of a nanosecond to several nanoseconds.

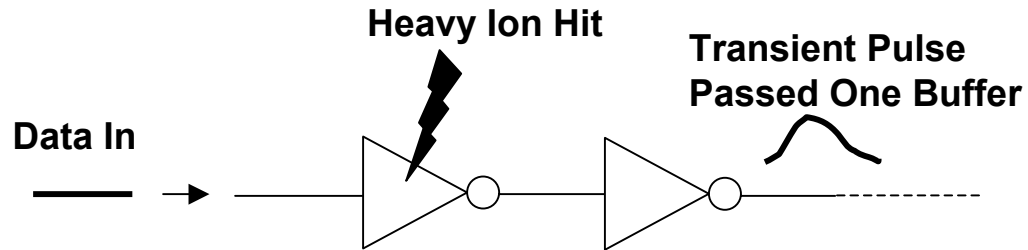
From Aerospace

Critical Transient Width vs Feature Size for Unattenuated Propagation



From Mavis

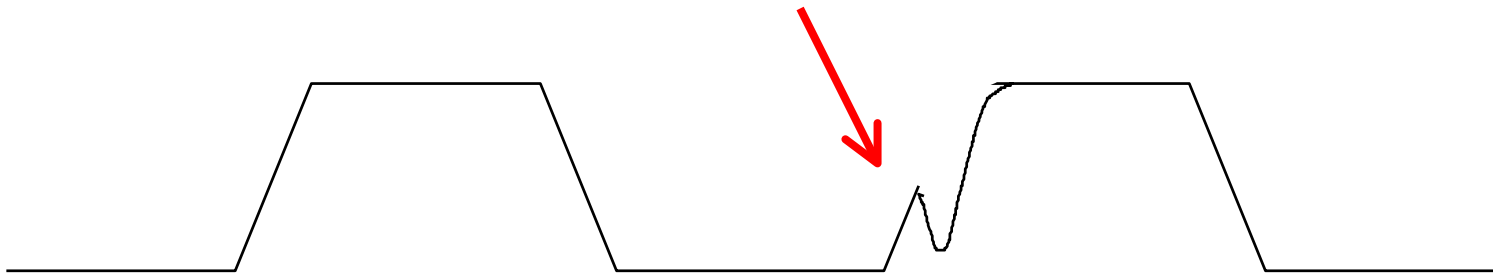
Mode 1 Transient Upset



- **Transient pulse higher than half VDC will propagate**
- **$Q_{crit} \sim 0.02\text{pC}$, or $LET_{th} \sim 2\text{MeV-cm}^2/\text{mg}$ for the worst case**

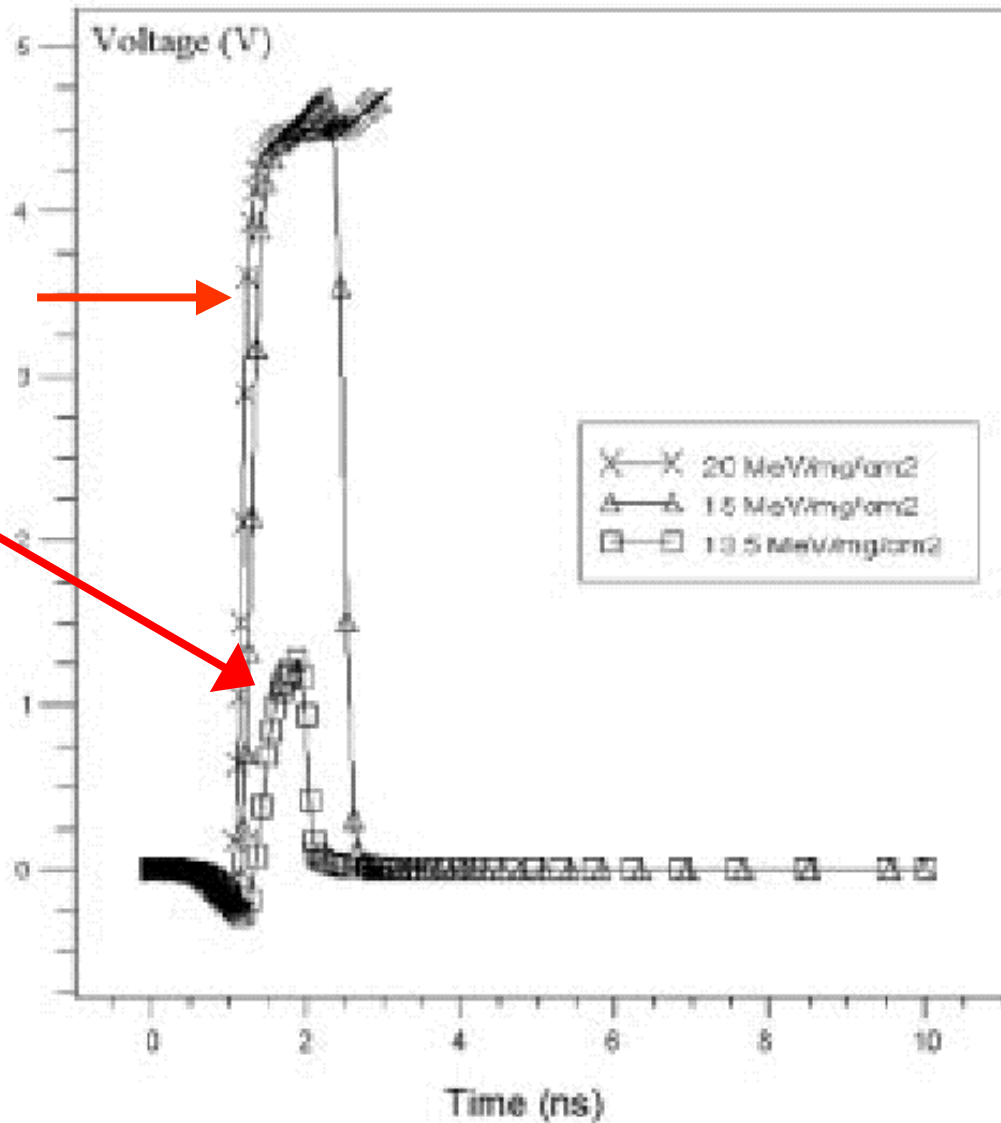
Double Clocking As a Result of Heavy Ion Induced Pulse

Heavy ion induced negative pulse



Cartoon of clock/logic upset. The device is most sensitive during the transition.

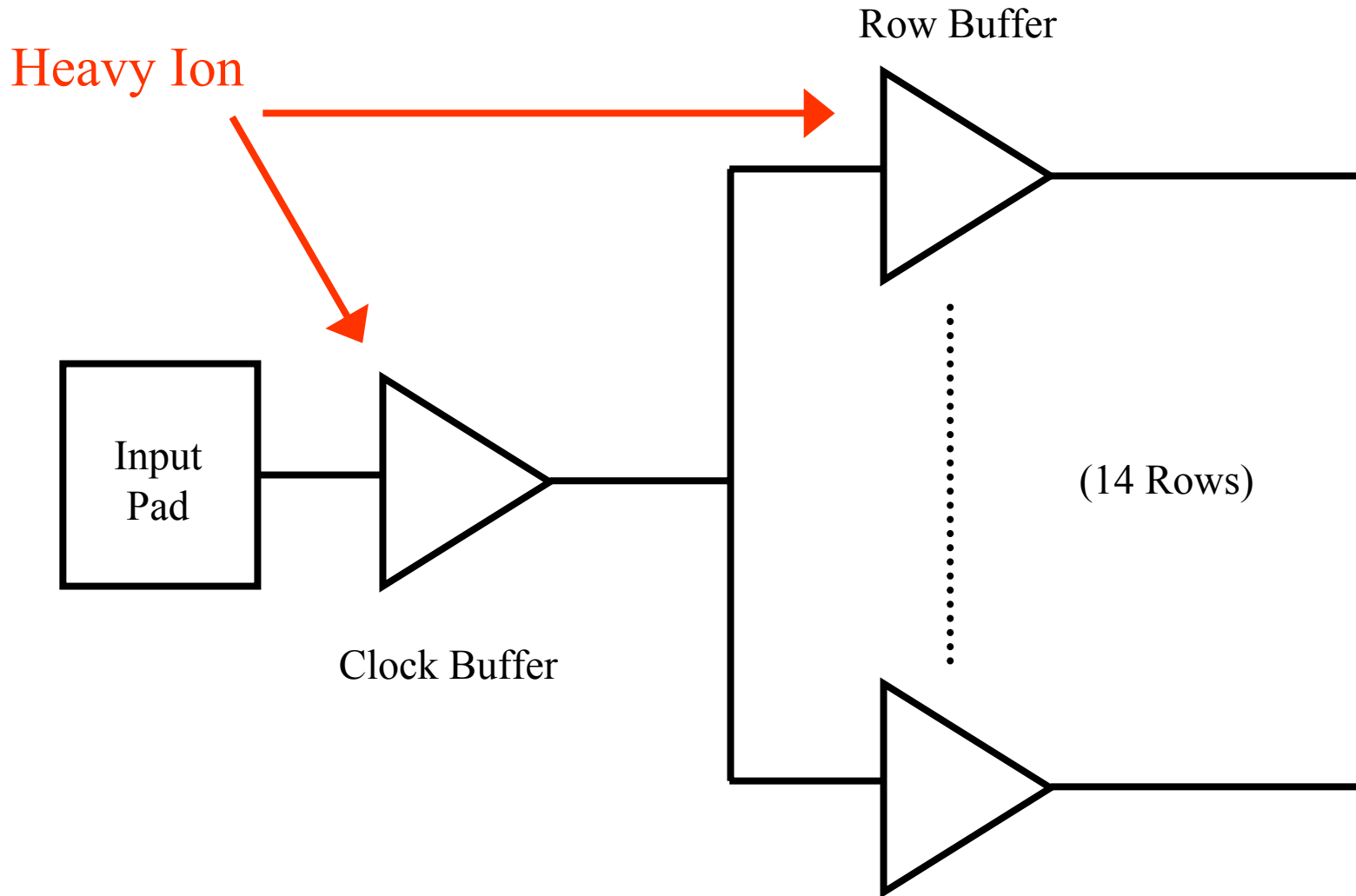
Simulated Upsets for Various LETs



Can get narrow and
runt pulses.

Clock Tree Buffers

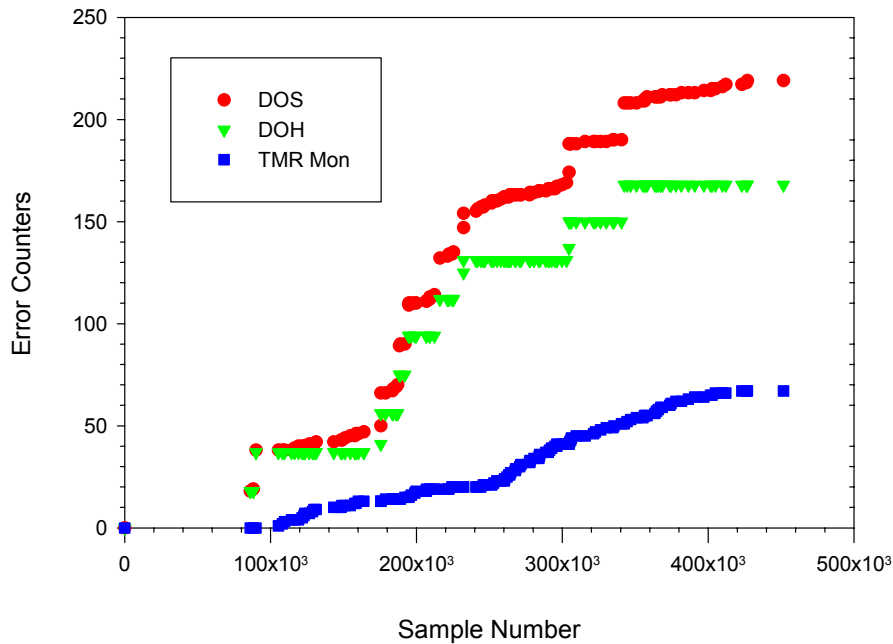
Sensitive to SETs



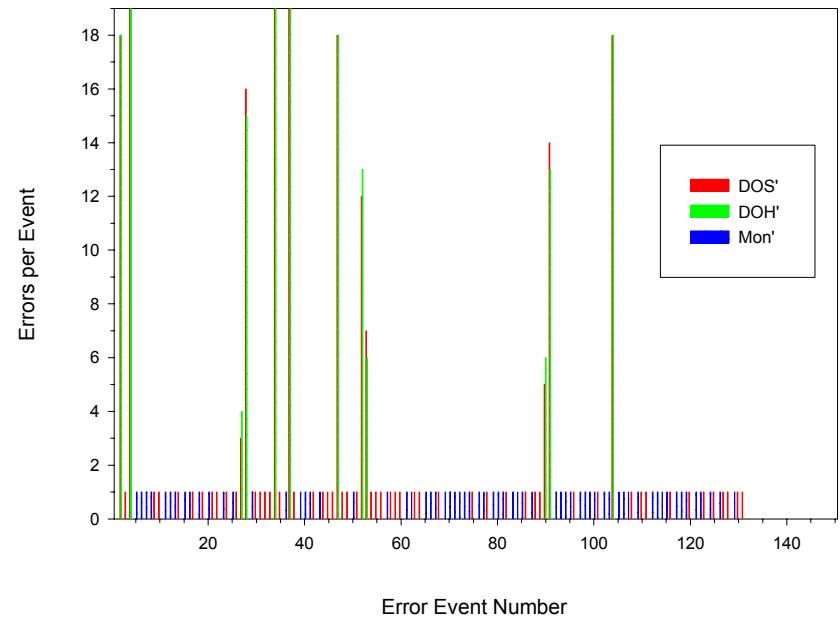
Clock Upset Instrumentation

1 MHz/Checkerboard

LET = 34.4

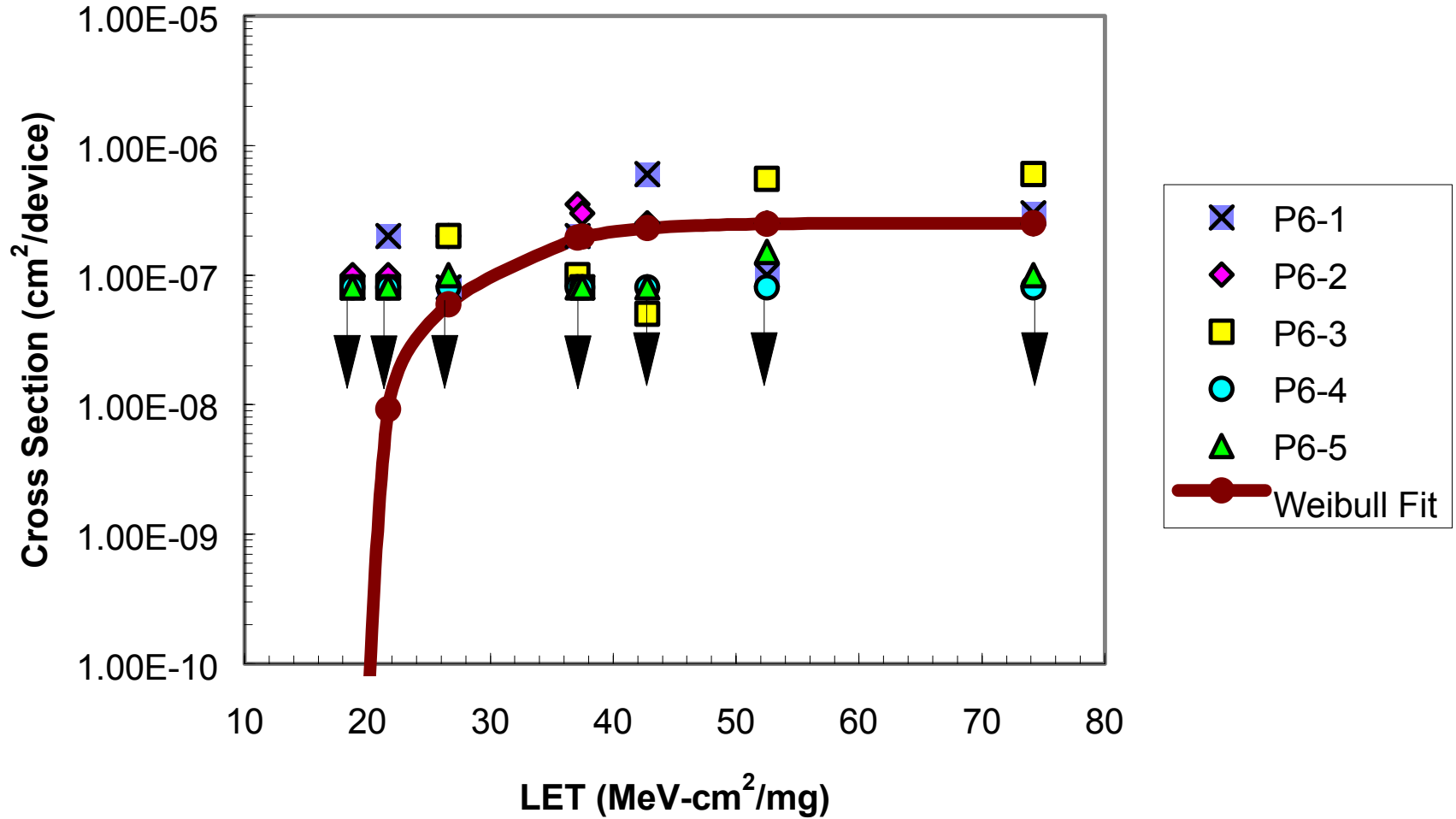


Cumulative Error Counts

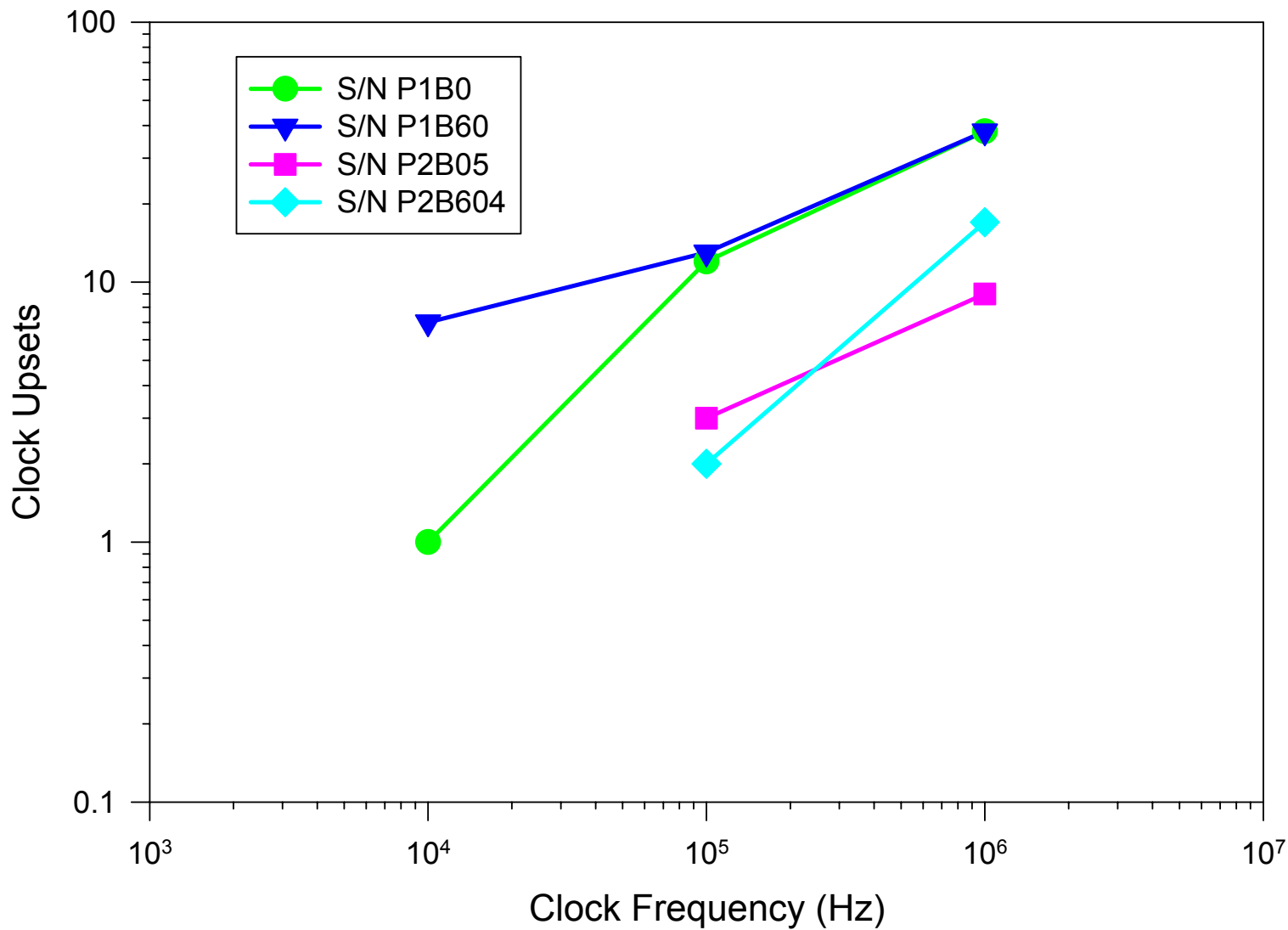


Differential Error Counts

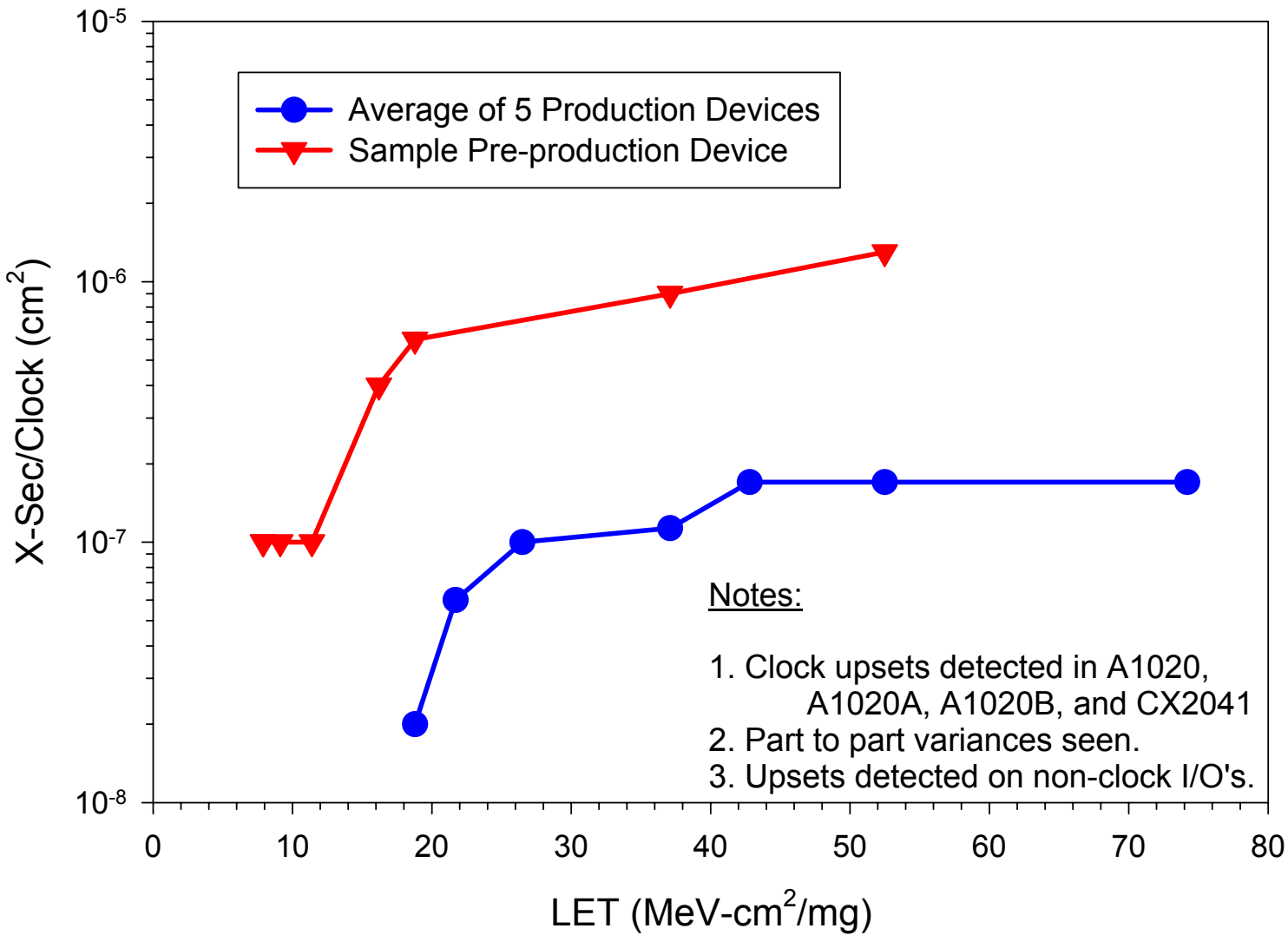
Clock Upset Cross Section



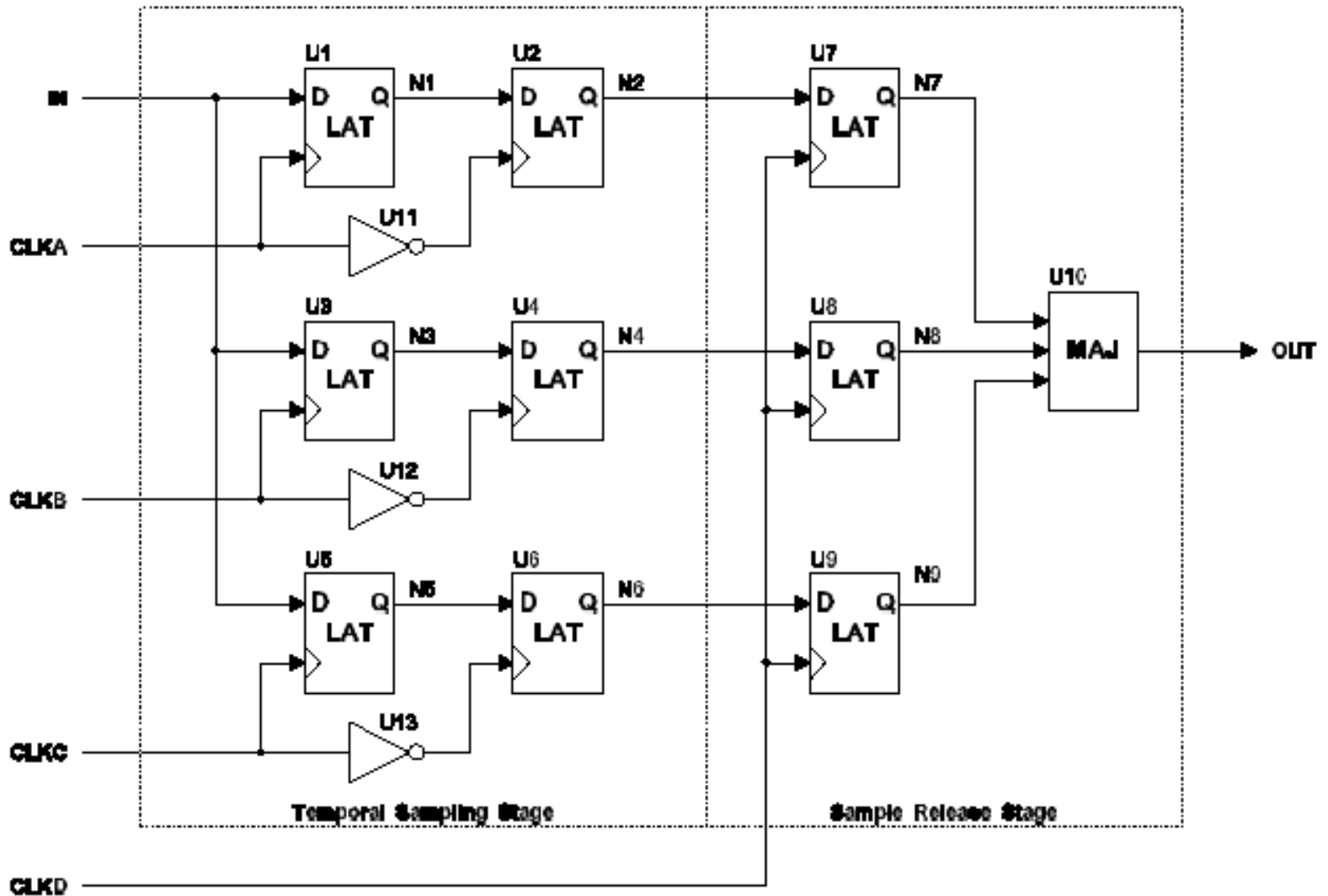
Frequency Dependence of Clock Upset



Clock Trees Can Be Hardened

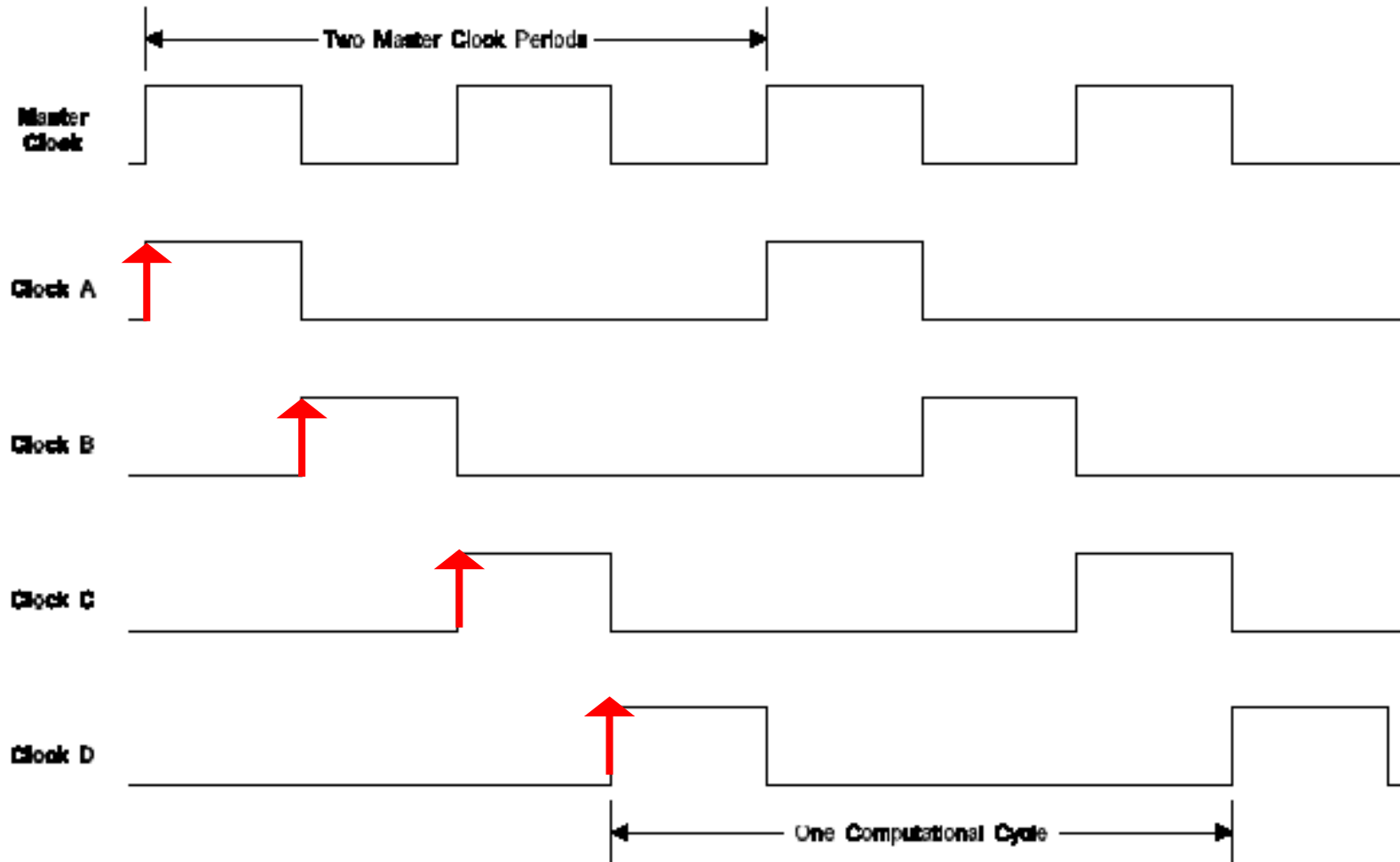


Temporal Sampling Latch with Sample and Release Stages



From Mavis

Temporal Latch Control Clocks Derived from Master Clock



From Mavis

Effects on Finite State Machines

- Can cause the equivalent of multiple bit error
- Can defeat parity, Hamming Codes, TMR, etc.

References

- "Clock buffer circuit soft errors in antifuse-based field programmable gate arrays, Jih-Jong Wang; Katz, R.B.; Dhaoui, F.; McCollum, J.L.; Wong, W.; Cronquist, B.E.; Lambertson, R.T.; Hamdy, E.; Kleyner, I.; Parker, W., IEEE Transactions on Nuclear Science, Dec., 2000.
- "Temporally Redundant Latch for Preventing Single Event Disruptions in Sequential Integrated Circuits," David G. Mavis and Paul H. Eaton, Mission Research Corporation, Technical Report P8111.29, September 1998 (revised October 1998).