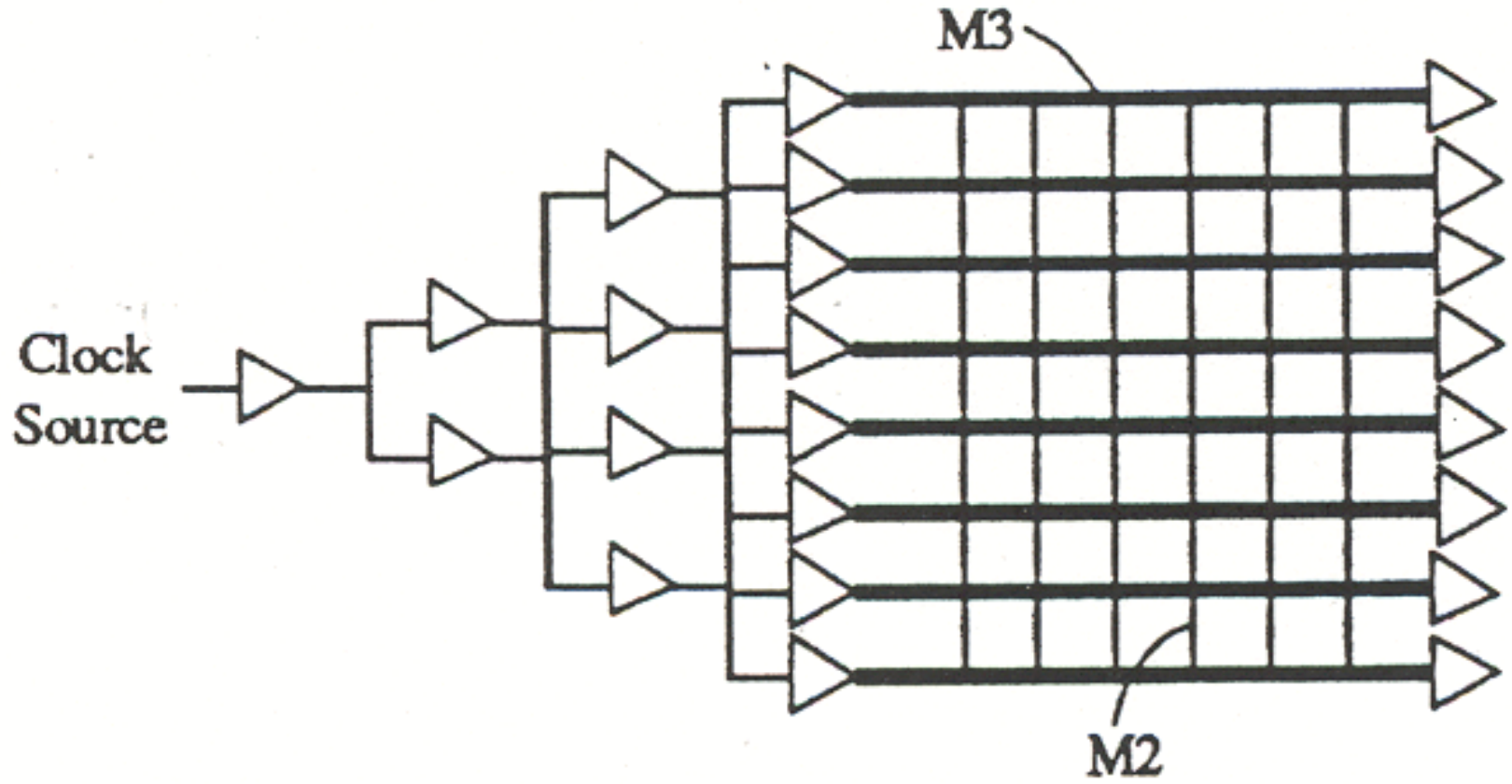


Microprocessor Clocking

DEC Alpha Clock Distribution



Case Study: Pentium 4

Core only; I/O not included

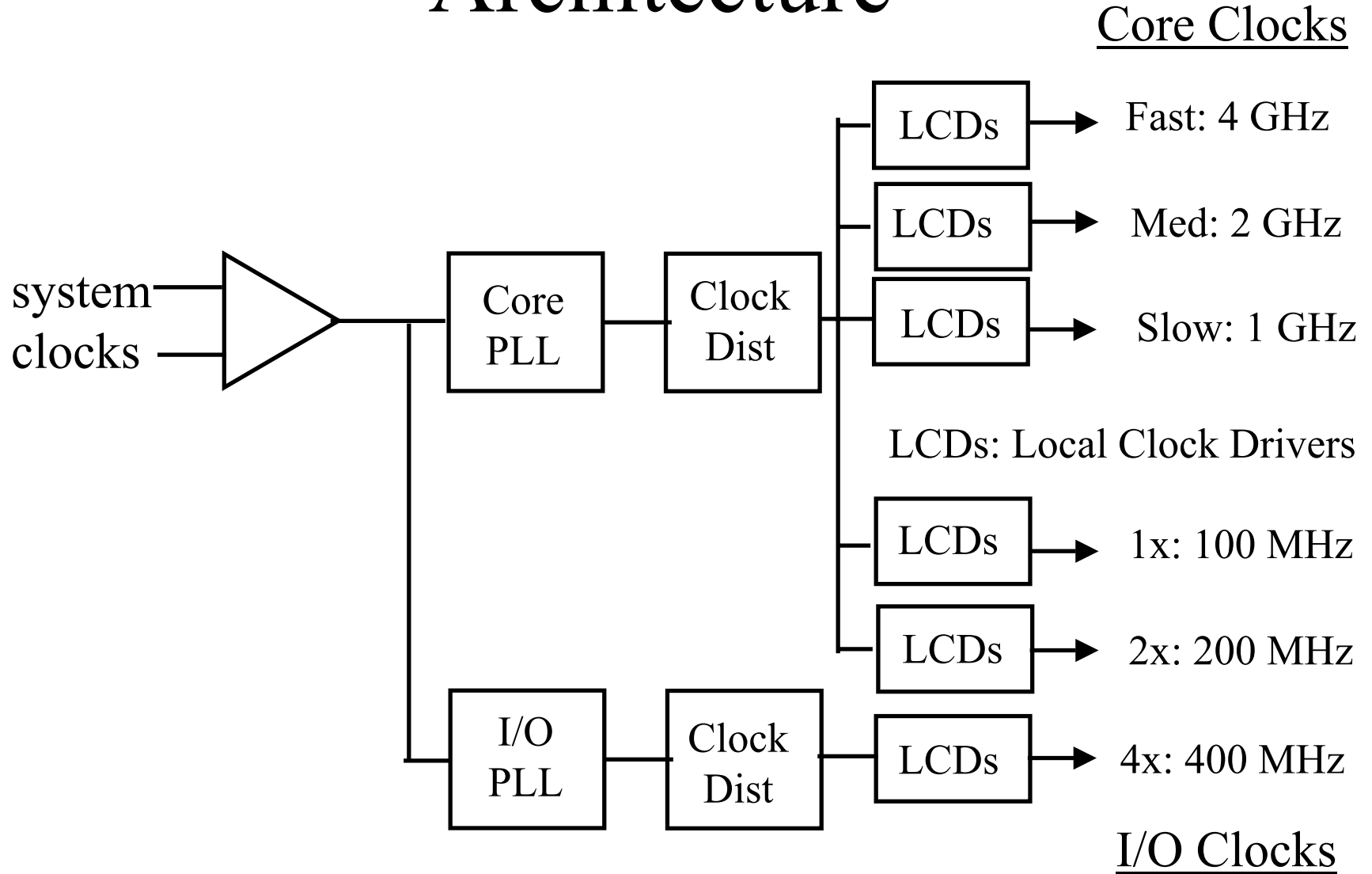
Pentium 4 Description

- Two PLLs
 - I/O
 - Core
- Clock Distribution Network
 - Skew optimized
 - Jitter reduced
 - ≥ 2 GHz core; ≥ 4 GHz rapid execution engine
- Pulsed and non-pulsed clocks
- I/O PLL has glitch detection and protection

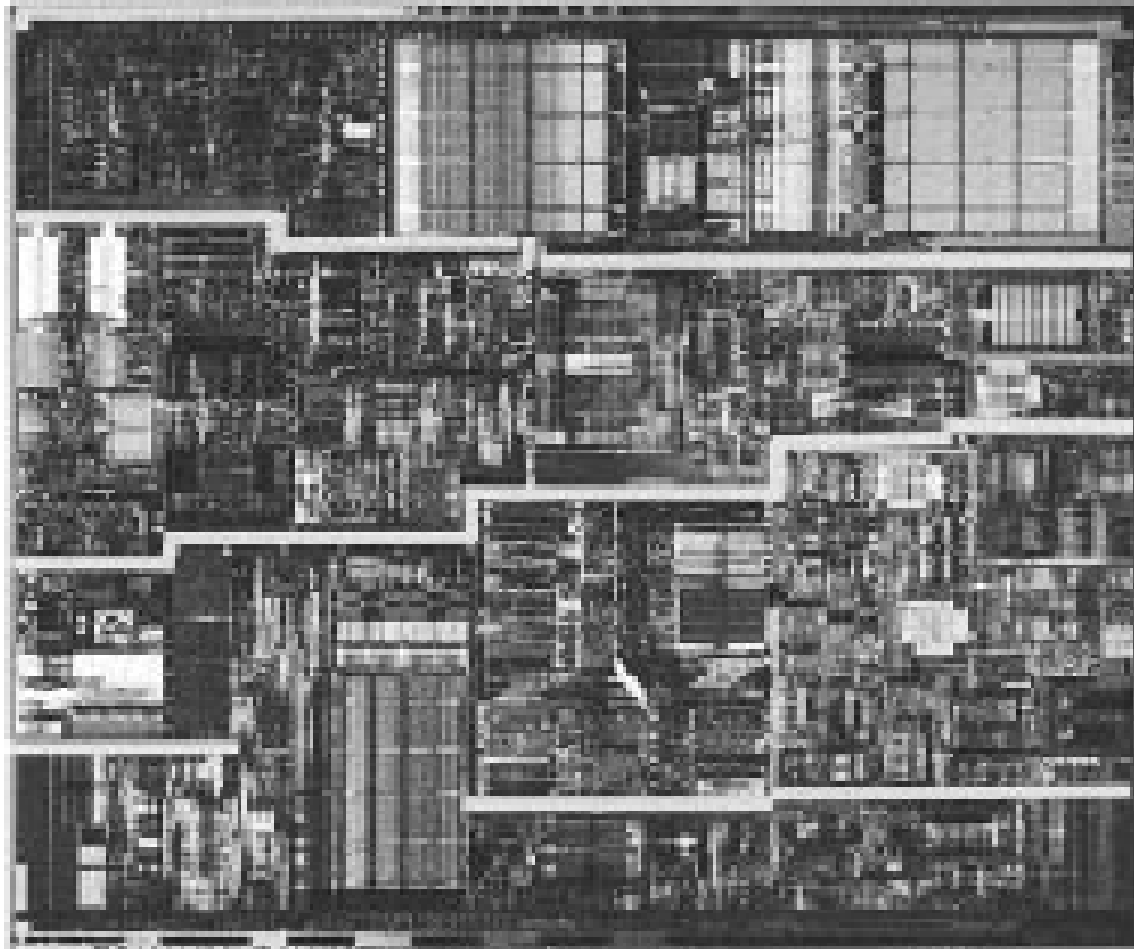
Pentium 4 Description

- 0.18 μm
- Six metal layers
- CMOS
- 42 million transistors

Architecture

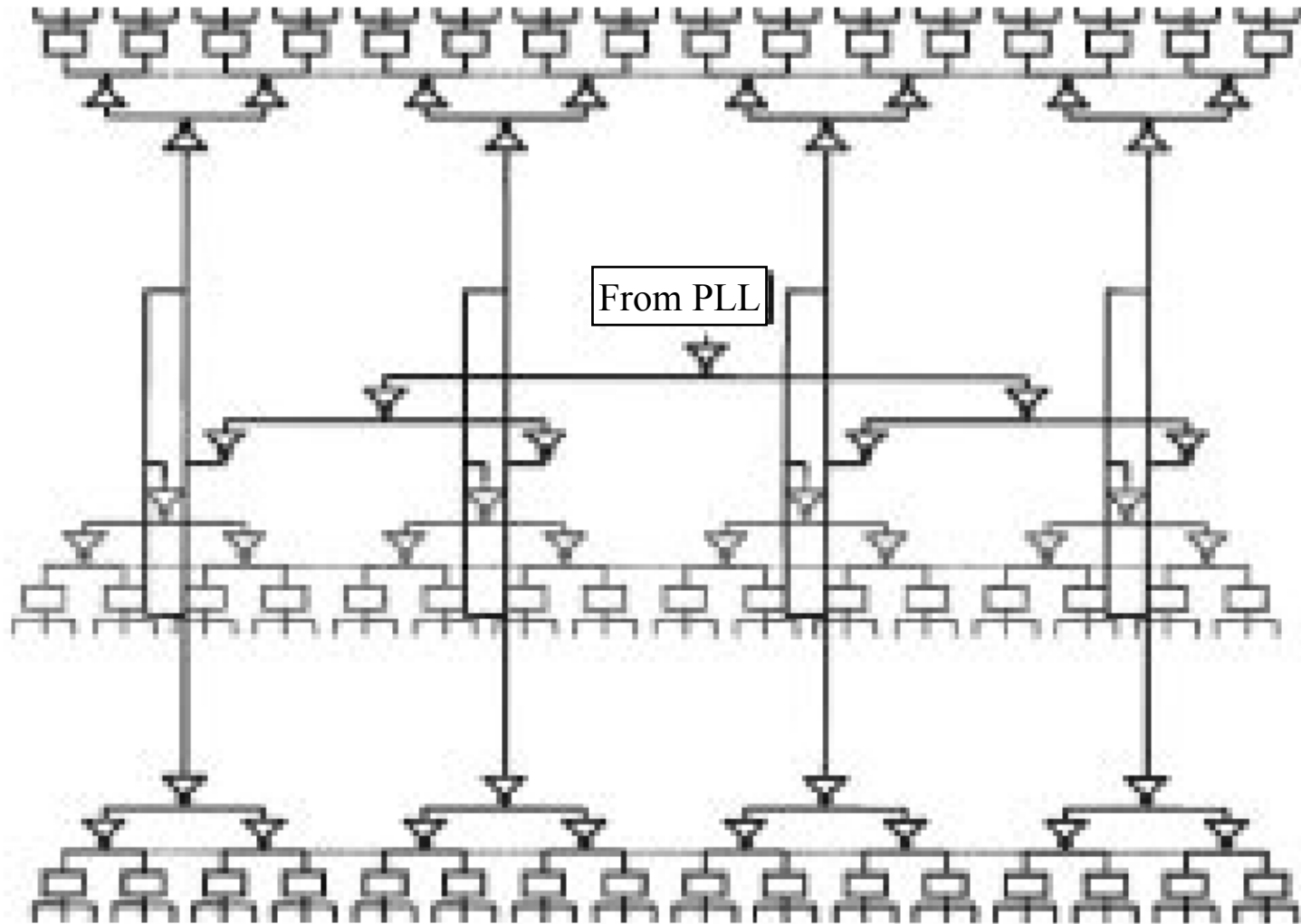


3 Clock Spines



Large die required 3 spines.

Binary Clock Distribution



Each leaf node is an independent clock domain

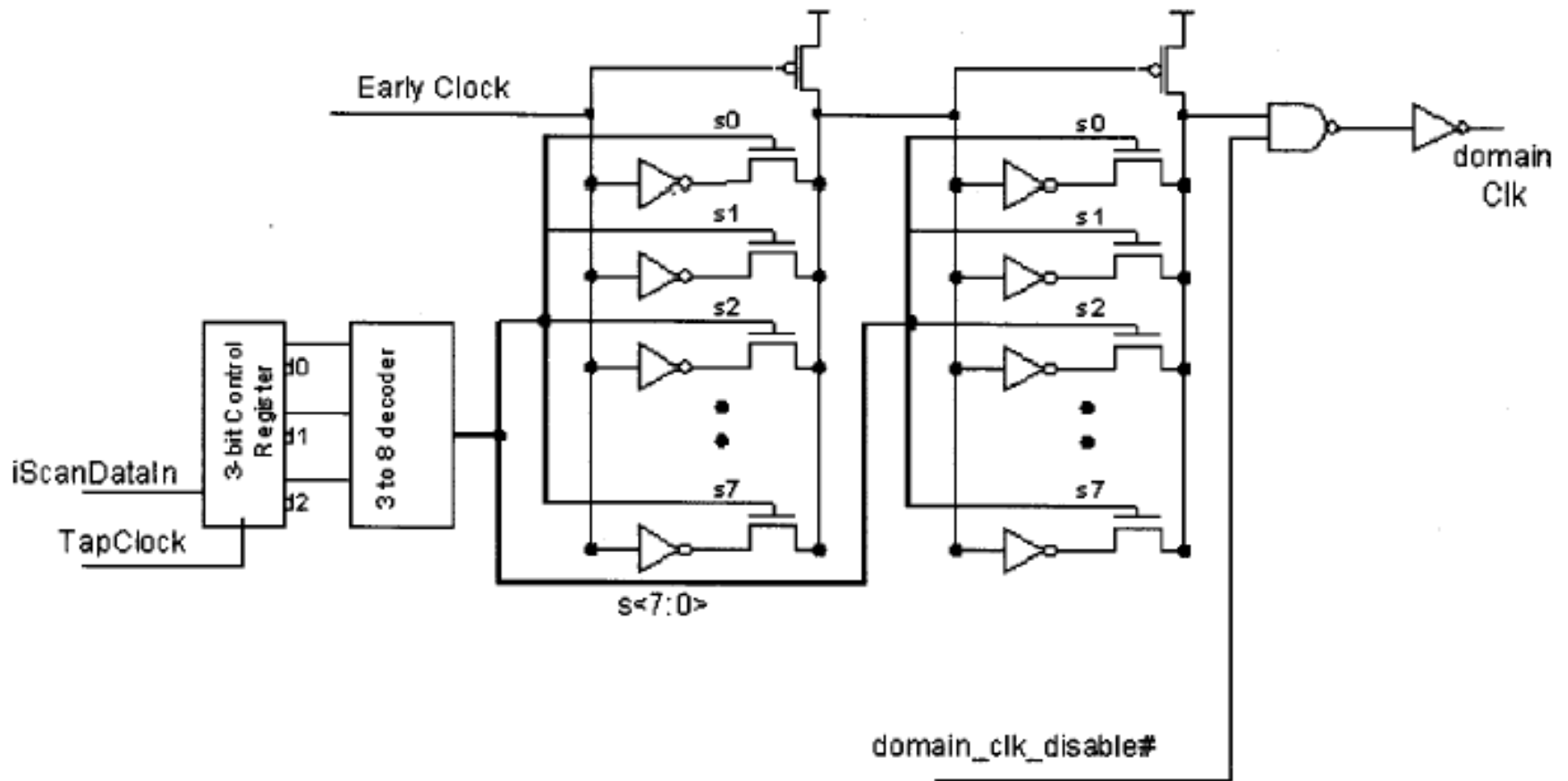
Systemic Skew

- Within-die Variations
 - Channel Length
 - Threshold
 - Width
 - Interlayer Dielectric Thickness
- Non-ideal Placement
- Modeling and Extraction Errors

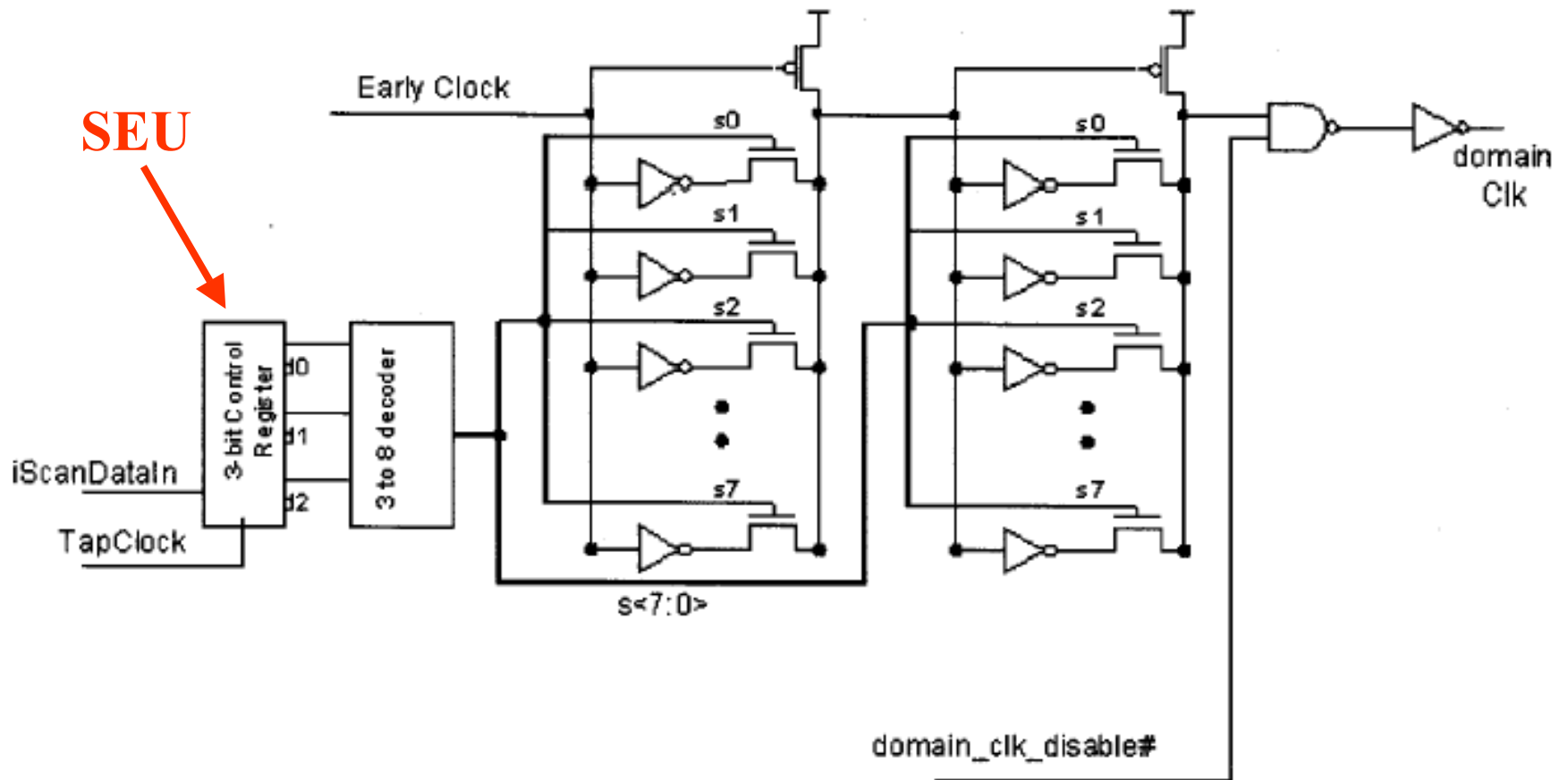
Skew Optimization

- 47 Adjustable Delay Domain Buffers
 - Accessible from a test access port
- Phase Detector Network
 - 46 Phase Detectors

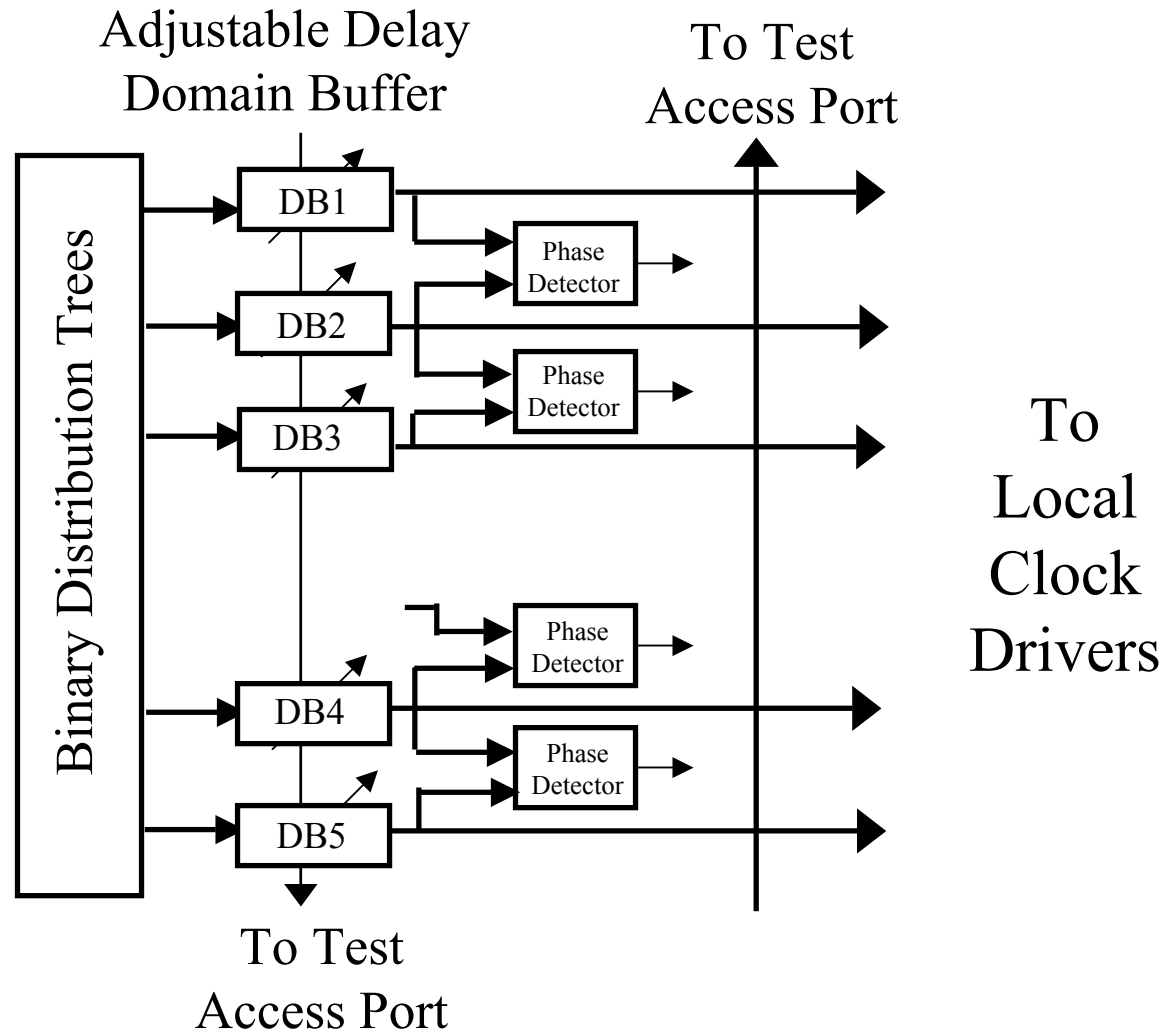
Adjustable Delay Domain Buffers



Adjustable Delay Domain Buffers



Skew Optimization Circuit



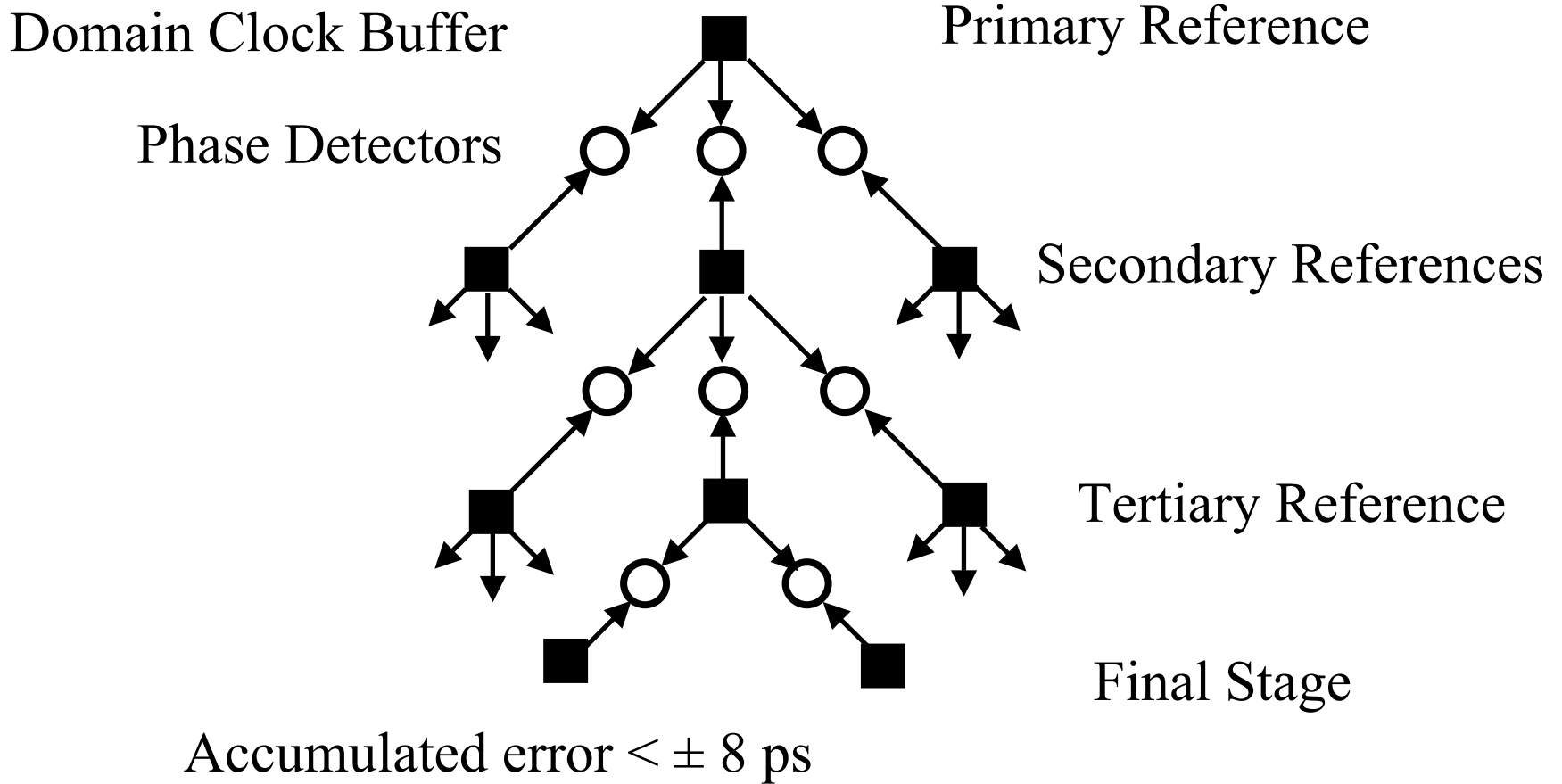
Skew Trimming

- Domain Buffer at the center of the die is the primary reference
 - Other levels: secondary, tertiary, final
- Secondary aligned to primary
- Then tertiary aligned to secondary
- Then final buffers aligned to tertiary level

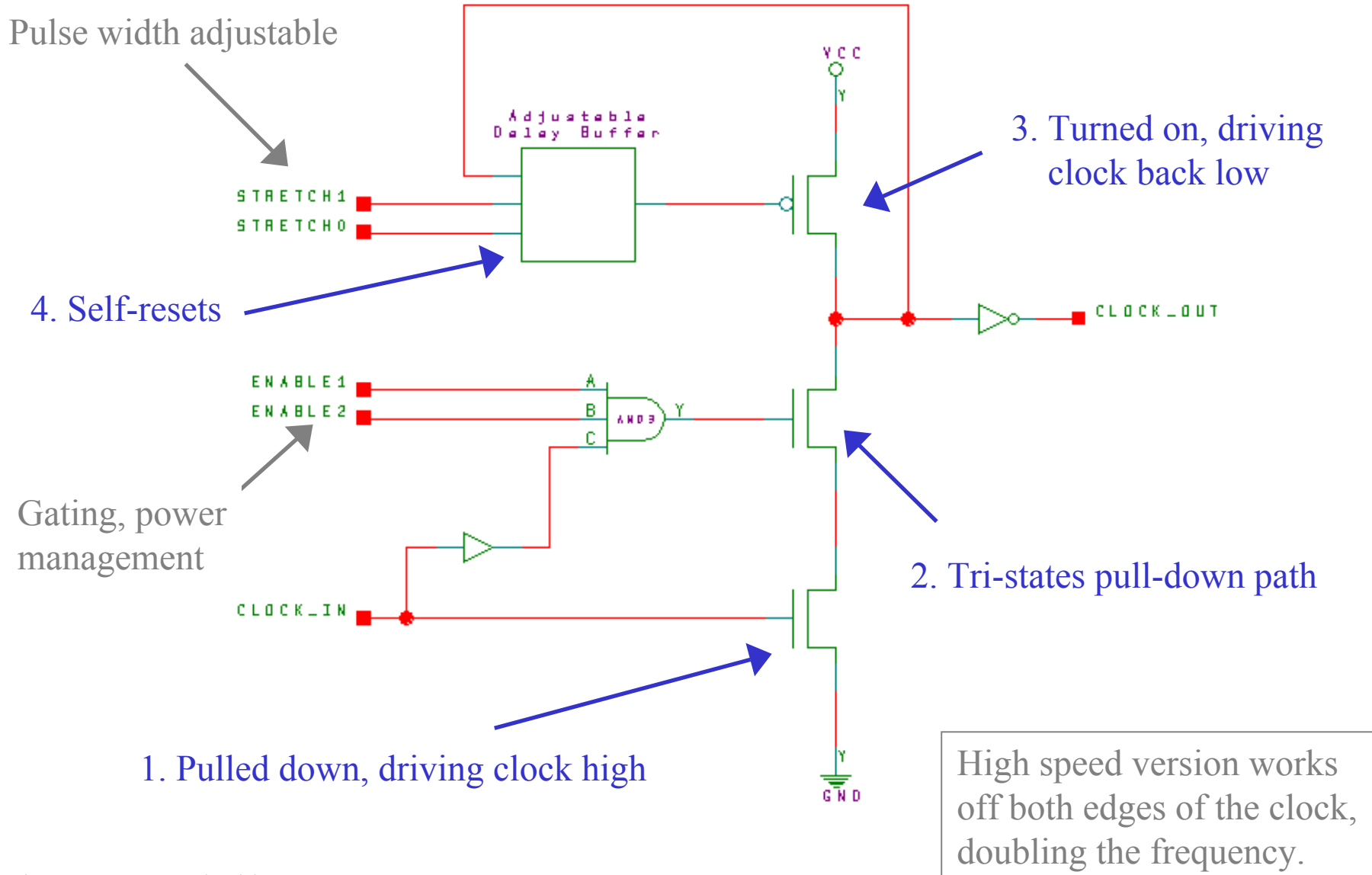
Skew Trimming (cont'd)

- Initial skew about 64 ps for a particular die
- Accumulated skew, after adjustment, about ± 8 ps
- Scheme can force deliberate skew
 - Improves performance, optimum pipelining

Skew Trimming (cont'd)



Medium Speed Pulse Generator



Pentium 4 Closing

- Presented basics of core clock distribution system
- Did not present:
 - Logic Design
 - I/O sections
- Exercise: Analyze SEU implications of the structures just discussed

Other examples available, add
when we get time

Itanium

AMD