

Designing Space Applications Using Synthesisable Cores

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Background

VHDL was adopted by ESA as the preferred HDL in the early nineties, then being the only standard and multi-vendor HDL.

VHDL model delivery were required for every ASIC developed, allowing ESA to independently verify the design by simulation.

ESA funded ASIC developments normally resulted in the delivery of prototypes or components integrated in equipment. It was difficult for competing companies to obtain the devices. The intellectual property (IP) rights belonged to the design house.

At that time Application Specific Standard Products (ASSPs) were introduced in ESA developments. The objective was to have the components distributed and supported by the manufacturing foundry, under fair and equal conditions for all European buyers. With each ASSP a VHDL model for board-level simulation was delivered. The IP rights still belonged to the design house.



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Background - Board-level simulation

Much effort was spent on perfecting VHDL models for board-level simulation, addressing aspects such as functional accuracy, simulation performance, and ease-of-use.

Difficult to establish an efficient distribution mechanism allowing companies to get access to models without giving away design information. Pre-analysed models were often distributed.

An approach to commercialising the models was attempted but failed due to poor interest from companies, not being willing to pay for maintenance etc.

Models have consequently been distributed free of charge by ESA to several companies who have been using them in both scientific and commercial spacecraft developments.

Good results were achieved with models that were made available freely on the net, provided with no or limited support from ESA.



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Background - VHDL cores

The previous ASSP concept included the protection of the foundries in a sense. The design of an ASSP was not open to other companies, avoiding multiple competing implementations of the same function since it would decrease the interest for foundries to support the devices as ASSPs.

However, with only a few European foundries offering space qualified process, the above approach has been partially abandoned. A board-level model is therefore not an important output from ESA funded ASIC/ASSP developments. Instead, synthesisable VHDL cores are now being requested.

The second reason for moving away from ASSPs to synthesisable VHDL cores is that the increased gate capacity of new space qualified technology has opened up the System-On-a-Chip arena for space applications. System houses are not integrating ASSPs any more, they are integrating cores instead.

Background - Managing VHDL cores

In a pilot ASIC development using and producing VHDL cores the following basic principles were laid down to manage the cores:

- Cores that are provided by ESA to the contractor should remain the property of ESA, including any modifications.
- Licensing rights for commercial cores that are purchased as part of the development should belong to ESA, with the right to sublicense the core to European space companies.
- For VHDL cores developed in the contract, ESA should be granted the ownership, with unlimited rights to distribute the core to European space companies.
- For existing VHDL cores belonging to the contractor, considered as background information, ESA should be granted the right to use them for in-house developments only.



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Developing VHDL cores

For each VHDL core that is required in ASIC developments a trade-off is being made between an in-house development, contracted development or purchase of a commercial core.

In many cases it has been considered important to have full and unlimited property rights to VHDL cores for certain key functions. These developments require specific in-house expertise.

The advantage of in-house developments is that the cores can be freely distributed on the net. There are no restrictions related to non-European users. The benefit is that a larger user base can be addressed, which can potentially provide vital feedback, allowing continuous improvement of the cores. The disadvantages are issues such as support, quality level etc.

The output from ESA developments are by default restricted to the member states, making distribution more difficult.

Completed VHDL core developments

The following VHDL cores are completed and currently available from ESA. Each core has been developed in-house, but current set up limits the distribution somewhat.

- **CCSDS Telemetry Channel Encoders:**
Reed-Solomon Encoder
Convolutional Encoder
Bundled with Packet Telemetry Encoder cores in a 20 kEURO package restricted to Europe. The next release will most probably not have this limitation.
- **VMEbus Controller (EVI32):**
Targeted to the ERC32 SPARC V7 chip set
Used by many non-European companies
Freely available on the net:
www.estec.esa.nl/wsmwww/erc32/evi32.html



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In-house VHDL core developments

The following VHDL cores are currently being developed in-house:

- **CCSDS Turbo encoder:**
Based on the updated CCSDS recommendation
Fits into an ACTEL1280 FPGA, using an external memory
Validation in progress
Mission foreseen in 2000-2001
No restriction on distribution since ESA property
- **CCSDS Packet Telemetry Encoder:**
New VHDL core optimised for multiple virtual channels using one external memory
Support for RS and Turbo encoders
ASSP foreseen in 2000-2001
No restriction on distribution since ESA property

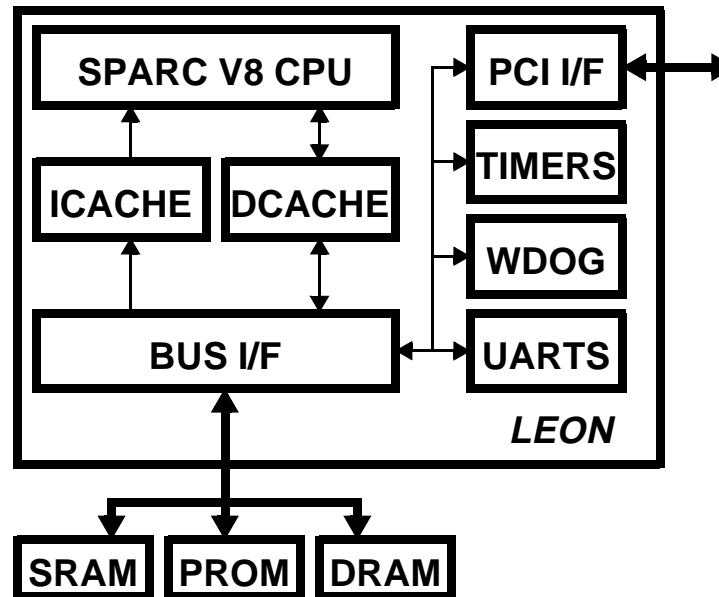


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In-house VHDL core developments, cont.

- **SPARC V8 (LEON):**
SPARC V8 based CPU with SEU protection and error handling
Will be freely available on the net (scaled down version)
Release this autumn



Industrial VHDL core developments

The following VHDL cores are being developed in industry. ESA will have the right to use and distribute the cores to European companies involved in developing ASICs for the space market.

- **CCSDS Packet Telecommand Decoder:**
The code from the development of an existing ASSP will be provided to ESA
The code has been validated in-flight
Limited to European developments under ESA contract
- **Wavelet Image Compression:**
Research development targeting a commercial process
Design written in C++, from which VHDL can be generated.
Core limited to space applications under ESA funding



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Planned VHDL core developments

The following VHDL cores are under development or are just being started up:

- **PCI Local Bus**
In-house development
Requires continuation covering verification and validation
Will be freely available when completed
Low cost alternative to commercial cores
- **CAN**
In-house development
Freely available
- **PSS-04-0255 Bus Terminal**
Initially available to European space companies
Industrial development, negotiations under way



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Purchasing VHDL cores

Quality level of VHDL code and documentation is not always complying to ESA standards.

Independent verification efforts have been made for a commercial core and three serious bugs were found. The core had been previously validated and used in commercial products!

Modifications for SEU protection etc. can be costly, often requiring a new verification or even validation.

Licensing issues are difficult to handle from ESA's point of view. ESA would like to buy the VHDL core once, but use it in multiple developments involving different companies. Two approaches discussed: ESA allowed to sublicense the core (ESA taking responsibility for contracting companies), ESA purchases the first core and subsequent buys are discounted (provider is handling contracting companies).



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Planned/Purchased VHDL cores

- **Intel 8032 compatible VHDL core**
The only purchased core so far (European provider)
ESA has the right to sublicense to European companies developing ASICs under ESA contract for the space market
- **PCI local bus**
Negotiation ongoing
Discount scheme foreseen
- **IEEE 1355**
Negotiations ongoing with European space company
- **IEEE 1394**
Development or purchase being considered
- **Mil-Std-1553**
Available from European source



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Developing FPGAs

Many of the benefits of using FPGAs in commercial applications often become a problem when applying the devices to space applications. FPGAs are perceived as easy to correct and modify late in the development process. This often leads to design methods that would not be accepted in ASIC developments.

ESA often receives equipment with FPGAs embedded for which there is no specific FPGA documentation, making it difficult to assess the correctness of the design. It becomes even worse when a problem is discovered late in the integration cycle and there is no visibility into the design or the verification process.

It is recommended that proper design methods are applied to FPGA designs, which will initially increase the FPGA development cost, but can reduce downstream costs in the long run.



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Developing FPGAs - Methodology

As for all design disciplines, proper specifications of each FPGAs should be established before implementation begins.

A verification plan should be established and implemented by someone else than the designers, to avoid error masking.

For generic FPGAs, the design should be validated beyond the obvious application cases to avoid problems when the design is used in a new environment.

Proper design methods should be applied: use HDLs even if performance might be better using gate pushing, make the design synchronous, include proper reset and initialisation, avoid bus contention etc.

Hold proper reviews and make room, in both FPGA and schedule, for potential redesign.



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Developing FPGAs - Documents

ESA ASIC and VHDL design recommendations available on-line:

- ***ESA VHDL Modelling Guidelines***
<ftp://ftp.estec.esa.nl/pub/vhdl/doc/ModelGuide.pdf>

Originally written for ASIC developments but most parts are relevant to FPGA design as well.

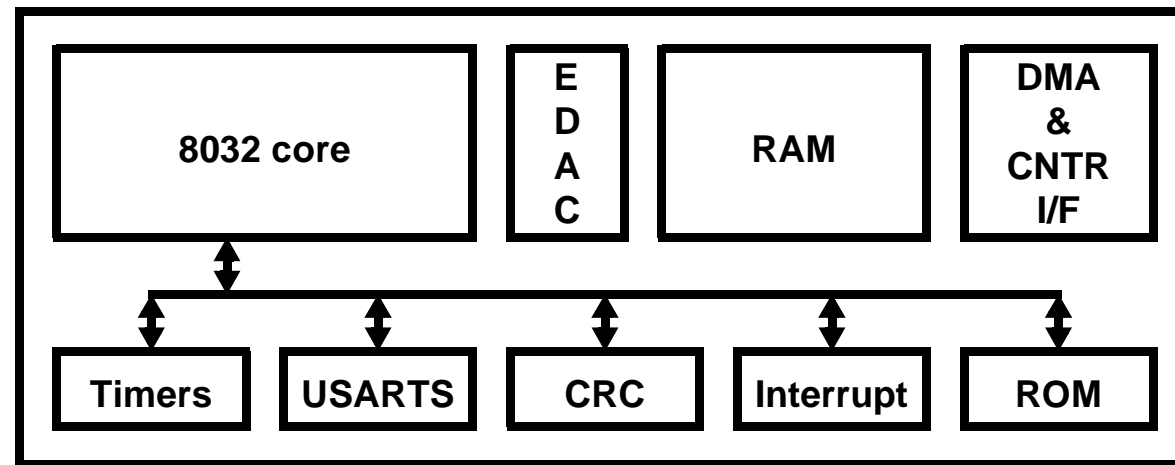
- ***ESA ASIC Design and Manufacturing Requirements***
<ftp://ftp.estec.esa.nl/pub/vhdl/doc/DesignReq.pdf>

Cover several issues related to HDL based design without being tied to any particular tool.

Developing FPGAs - Using VHDL cores

The first ESA funded attempt using cores when designing a flight FPGA was done with an 8032 core.

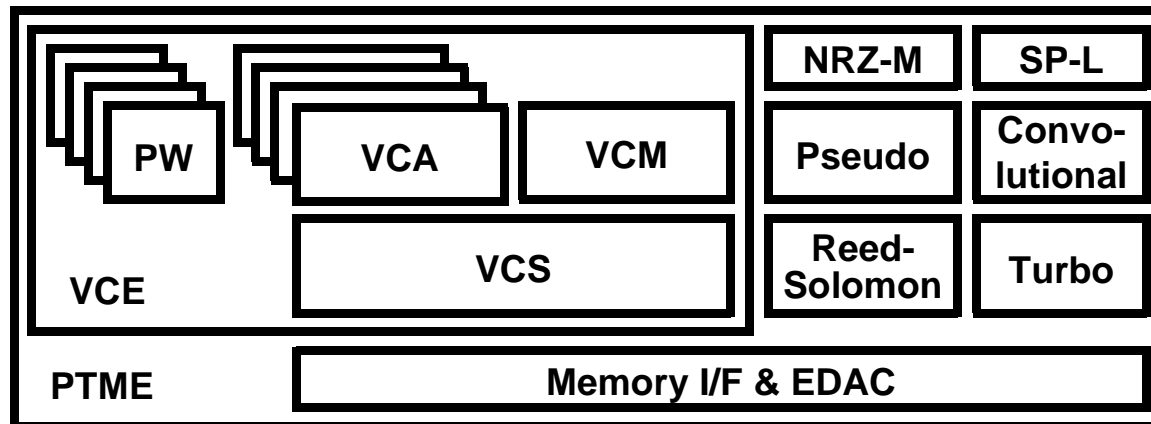
The lesson learned is that the selected FPGA was too small, in fact three components were needed in the end. Since flight worthy FPGAs are too small for our application, it was decided to implement an ASIC instead, featuring additional functions.



Developing FPGAs - Using VHDL cores, cont.

The first in-house development using cores is based on the CCSDS packet telemetry and channel encoder cores developed at ESA. Lesson learned is that adaptations specific to the FPGA technology limitations need to be considered, which ultimately requires time and resources for both implementing and verifying.

Reuse of code that not written with such a purpose in mind can be more difficult than to begin from scratch. The verification plan and testbenches are always useful, even if not always easy to use.



Developing FPGAs - Experiences

FPGAs have been used in many ESA developments, ranging from breadboards to flight equipment, with a mixture of success stories and problem cases.

One bad example is when a function was validated using FPGAs which were subsequently transferred to an ASIC on the gate-level. This introduced problems in layout etc. and resulted in many bugs.

Another bad example is when multiple FPGAs were to be merged into one ASIC which should be configurable to operate as either FPGA at a time. The benefit would be simpler qualification, procurement, and lower power consumption etc. The schedule slipped since many of FPGAs were not completed or validated, which resulted in abandoning the ASIC development and flying FPGAs instead. FPGA prototyping is not always a guarantee that your ASIC development will be successful.



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Developing FPGAs - Experiences, cont.

The more successful cases have been related to dedicated FPGA developments, implementing a specific function.

One example is the three FPGA based cameras that were mounted on the TeamSat satellite and used for observing the separation between the spacecraft and the launcher.

For the same spacecraft, an ESA in-house development of the data handling system included two FPGAs that were developed from scratch based on proper specifications and verification using board-level simulation. Both FPGAs were first time right and were located strategically in the up- and down-link of the communications system.



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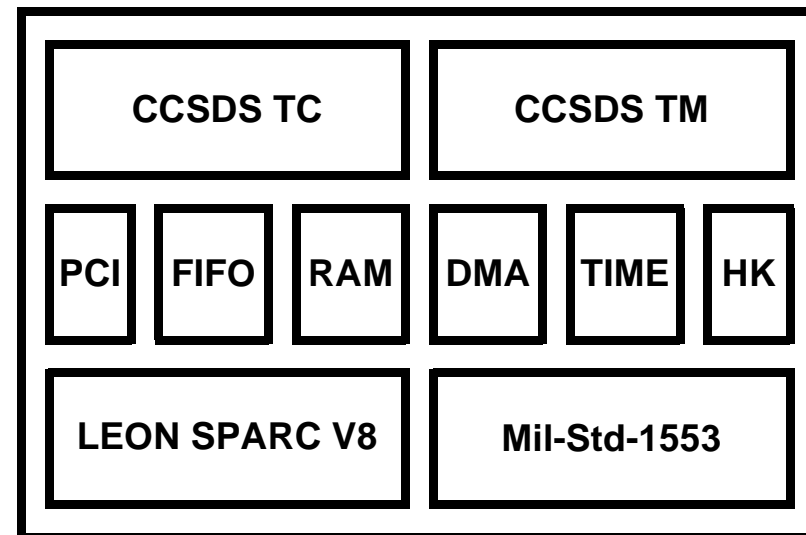


Developing a SOC using VHDL cores

VHDL cores are being used in a pilot SOC demonstrator development under ESA contract. A complete data handling system is being designed on a single device. The design is almost entirely based on cores or reuse of existing building blocks. The device is expected to comprise some 300 kgate and 300 kbits on-chip memory, currently targeting a commercial standard cell technology.

Although FPGAs are used for prototyping some blocks, it is generally not possible to use current flight worthy FPGAs for such complex critical systems.

Both in-house, commercial and company specific cores are used in this development.



Conclusions

ESA is actively developing and using cores, both in-house and in industry. It is however expensive to develop high quality cores. It is not enough just to reuse code from previous developments.

It is as expensive and time consuming to purchase cores. Much effort has been spent on verifying the correct functionality of commercial cores, with many bugs being discovered.

Modifications are sometimes necessary to deal with SEUs etc.

Licencing issues will always be difficult if overall savings are to be made. Sublicencing / discount schemes are being negotiated.

The use of synthesisable cores in flight worthy FPGAs is limited by the low complexity of the devices, often leaving no space for application specific functions next to the core itself.

Great potential for cores lays in SOC applications, facilitating system level design.



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