An FPGA Based Adaptive Computing Implementation of Chirp Signal Detection

R. Bassett, J. Zaino, T.S. Sun,
J.M. Smith, E. Pauer, S. Kintigh
Sanders, A Lockheed Martin Company
Nashua, NH 03061-0868
john.c.zaino@lmco.com

D.W. Tufts
Univ. of Rhode Island
Kingston, RI 02881
tufts@ele.uri.edu

Abstract

Under the AFRL/DARPA Adaptive Computing Systems (ACS) “Reconfigurable Algorithms for Adaptive Computing” (RAAC) program, Sanders, A Lockheed Martin Co. is investigating innovative algorithms that are applicable to the signal processing of digitized RF signals including electronic warfare (EW) operations suitable for field programmable gate array (FPGA) implementation. The latter has been identified as one of the most promising enabling hardware technologies for advanced adaptive computing system realization. Many RF systems and in particular EW systems have two major operational requirements: the detection of electromagnetic emissions and the demodulation or measurement of their characteristics. The criteria for assessing any particular algorithm design are thus based on performance with respect to these operational requirements as well as its efficiency with respect to FPGA implementation. This paper describes the implementation of a technique for linear FM chirp signal detection on a COTS FPGA based reconfigurable computing testbed. The scheme used for signal detection is based on a semi-coherent method originated by Lank, et al[1].

The scheme we have demonstrated addresses, in an adaptive computing environment, the detection of a family of signals that can be hard to detect at reasonable false alarm rates. When viewed by a receiver that simply looks for energy in the frequency excursion band of interest the SNR (signal to noise ratio) of many of the signals of interest are very low or negative. Such signals are undetectable without further processing. The techniques we have demonstrated make it possible to enhance the detection and measurement SNR by 10 to 20 dB (depending on signal pulse widths and excursions) and to process incoming data at real time rates in excess of 30 Million samples per second.

The semi-coherent technique for signal detection was one of three signal processing schemes studied using analytical models as well as Monte-Carlo type simulations. These studies were aimed at defining the optimal operational boundaries of each scheme vs.defining which scheme was the best design choice. This will allow a reconfigurable design strategy to be developed to exploit the full potential offered by the adaptive computing architecture.

The semi-coherent method consists of two parts: a preprocessing step which involves a sample-by-sample multiplication of the received signal with the complex conjugate of a delayed copy, and an FFT spectral analyzing step. We have implemented the pre-processing step of this scheme in an FPGA using and extending tools developed on the (DARPA ACS) Algorithm Analysis and Mapping Tools program, including coupling of data between Ptolemy (the design environment used for the Algorithm Analysis and Mapping Tools program), Matlab and a DoD Signal Processing Analysis package. The result was a powerful approach to rapid iterative ACS algorithm analysis and visualization using popular commercial tools and confirmation of results in end user preferred formats.

---

[1] G.W. Lank, I.S. Reed, and G.E. Pollon, “A Semicoherent Detection and Doppler Estimation Statistic”, IEEE Trans. Aerospace and Electronic Systems, Vol. AES-9, pp. 151-165 (1973).

“This material is based upon work supported by the AFRL/Information Directorate under Contract No. F30602-98-C-0104. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the AFRL/Information Directorate.”

We have illustrated the performance potential of Adaptive Computing technology in high bandwidth data streaming applications, using a hybrid FPGA and FFT data streaming architecture to accomplish a function and data rates conventionally achieved only in analog applications. From a modular view, the results illustrate the ability of a single chip ACS implementation to perform the core function of a 9x9 inch conventional analog digital technology module while reducing power requirements from 70W to less than 3 W.

“This material is based upon work supported by the AFRL/Information Directorate under Contract No. F30602-98-C-0104. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the AFRL/Information Directorate.”