

Analog Module Architecture for Space Qualified Field Programmable Mixed Signal Arrays

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Abstract:

The ability to use radiation-tolerant programmable digital logic parts in hardware intended for use in high-reliability space missions provides significant cost savings. The savings result partly from shorter design cycles and lower risk, but mostly from reduced parts acquisition and flight qualification costs. Without these parts, many projects would be unable to afford custom gate array implementations, and would be forced to resort to discrete designs with the accompanying increase of system size, mass, and power consumption.

A similar situation exists in the mixed-signal field today. Almost all spacecraft and military systems contain numerous circuits which require moderate-performance analog and digital processing and I/O. These circuits are widely distributed throughout the system hardware, used for applications such as status monitoring, motor and temperature control, and signal conditioning and processing.

Until now, these mixed-signal circuits have been implemented almost exclusively using discrete parts, because the cost savings are not significant enough to justify a custom ASIC design. However, the resources used by such circuits, including mass, power, and volume, add up very quickly. The ability to implement such designs using a general-purpose, programmable mixed-signal array (FPMA) would be very welcome. The advantages of using an FPMA would be similar to those of an FPGA, namely much lower parts acquisition and qualification costs, higher levels of integration, lower power, and fast turn-around design cycles. It would also provide an improvement in overall reliability.

A field programmable mixed-signal array comprises digital, analog, and interface modules. This paper considers the electronic architecture of the analog modules for implementation in a CMOS technology with high quality antifuse interconnects. VLSI fabrication processes for which antifuses are available are digital processes used by the FPGA industry, and some meet the stringent requirements of radiation tolerance for spaceflight applications. However, they are not well suited to traditional analog design, and so necessitate careful considerations for the implementation of analog circuits in a digital process. Fortunately, this aspect of analog design has been a primary focus of

research in recent years due to the wide availability of digital processes and the shrinking availability of dedicated analog processes. A major constraint of analog VLSI design is the requirement for linear capacitors. FPMAs add the constraint that fabricated capacitors have a large capacitance per unit area, so that a sufficient number of programmable capacitor arrays (PCAs) will fit on a single chip of area comparable to standard FPGAs.

The lack of a dedicated analog process restricts the analog part of the FPMA implementation to switched-capacitor designs. While the nature of switched-capacitor circuits may prevent their use for some high-bandwidth applications, the use of low-resistance (on the order of 25Ω) antifuse interconnects significantly extends the range of applications for which switched-capacitor circuits can be used. Recent research¹ on switched-capacitor designs for field-programmable analog arrays provides us with fast and efficient array designs. Other research² provides circuits and layout considerations for linear capacitors in a digital process when used in a switched-capacitor framework. All indications are that the coupling of high-speed switched-capacitor FPAA designs with analog techniques for digital processes will produce viable programmable chips to meet the needs of spacecraft designers.

¹E. K. F. Lee and W. L. Hui, "A Novel Switched-Capacitor Based Field-Programmable Analog Array Architecture," *Analog Integrated Circuits and Signal Processing*, **17** (1,2), September 1998.

²H. Yoshizawa, Y. Huang, P. F. Ferguson, Jr., and G. C. Temes, "MOSFET-Only Switched-Capacitor Circuits in Digital CMOS Technology," *IEEE Journal of Solid-State Circuits*, **34** (6), June, 1999.