

FPGA Implementation of Sine and Cosine Generators Using the CORDIC Algorithm

Tanya Vladimirova and Hans Tiggeler

Surrey Space Centre

University of Surrey, Guildford, Surrey, GU2 5XH

Tel: +44(0)1483 879137

Fax: +44(0)1483 259278

email: T.Vladimirova@ee.surrey.ac.uk, H.Tiggeler@ee.surrey.ac.uk

Abstract:

The **CO**ordinate **R**otation **D**igital **C**omputer (CORDIC) algorithm is a well known and widely studied method for plane vector manipulation. CORDIC computation adopts only primitive arithmetic operations – algebraic addition and shift - instead of multiplication. The CORDIC algorithm has become a widely used approach to elementary function evaluation when the silicon area is a primary constraint. The main drawback is the intrinsic low performance due to the iterative nature of the algorithm. Many modifications of the algorithm have been suggested to improve its performance [1,2,3].

While there are numerous papers covering various aspects of the CORDIC algorithm, very few concentrate on implementation in FPGAs [4].

The aim of this paper is to propose CORDIC schemes for fast and silicon area efficient computation of the sine and cosine functions that are suitable for FPGA-based implementation. The results of theoretical investigation into different CORDIC schemes for fast computation of sine and cosine will be presented. Summary of VHDL coding and simulation of selected CORDIC algorithms for sine and cosine will be given. The resultant implementations will be analysed and compared. The specifics of the FPGA implementation medium in terms of constraints and resources will be discussed.

Finally, the paper will discuss approaches to incorporating CORDIC sine and cosine generators in small satellite on-board computer systems for specialised digital signal processing tasks.

References:

1. S.Wang, V.Piuri. A Unified View of CORDIC Processor Design – in “Application Specific Processors”, ed. By Earl E.Swartzlander, Jr, Ch5, pp.121-160, Kluwer Academic Press, November 1996.
2. M.D.Ercegovac, T.Lang. Fast Cosine/Sine Implementation Using CORDIC Iterations – IEEE Transactions on Computers, Vol.40, No.9, pp.222-226, 1987.
3. D.Timmermann, H.Hahn, B.J.Hostika. Low Latency Time CORDIC Algorithms – IEEE Transactions on Computers, Vol.41, No.8. August 1992.
4. R.Andraka. A Survey of CORDIC Algorithms for FPGA Based Computers – Proc of the 1998 CM/SIGDA Sixth International Symposium on FPGAs, February 22-28, 1998, Monterey, CA, pp.191-200.