Effective Implementation of a Generic Wavelet Filter on a Hybrid Reconfigurable Computer

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Hybrid Reconfigurable Computing Environment is one of the first general-purpose reconfigurable machines combining the flexibility of traditional microprocessors with the power of Field Programmable Gate Arrays (FPGAs). In this environment, computations can be divided into those executed in software, using instructions of microprocessors, and those executed in reconfigurable hardware, using capabilities of modern FPGAs. The programming model is aimed at separating programmers from the details of the hardware description, and allowing them to focus on an implemented function. This approach allows the use of software programmers and mathematicians in the development of the code, and substantially decreases the time to the solution. The SRC-6E Reconfigurable Computer is an example of this category of hybrid computers.

The Hybrid Reconfigurable Computing environment provides a programmer with the flexibility necessary to exploit various architectures that can be used to implement the same function. The choice among these architectures can be done at the level of a high-level language, such as C, FORTRAN, VHDL/Verilog and, schematics diagrams.

Digital Image processing is a rapidly evolving field with growing application in science and engineering. Image processing algorithms can be classified into Image Enhancement and Image Analysis. Generally image enhancement algorithms produce modified images as output, intended for subsequent analysis by humans or machines. On the other hand Image Analysis produces information which is much smaller in quantity but much more highly refined.

Until recently the computational burden of digital image processing for the most part had to be handled by dedicated hardware. Typically such hardware consisted of plug-in cards for PCI and/or VME backplanes, containing one or more Application-Specific Integrated Circuits (ASICs) designed for digital image processing. The last decade has seen a move away from dedicated hardware towards pure software solutions, due to the advent first of DSPs and later general-purpose computers.

In this paper we will investigate the effectiveness of combining the power of both realms (Generality of Software and the Speed of Hardware) by using Hybrid Reconfigurable Computers. These platforms allow us to implement generic image

processing kernels, which can be used for both Image Enhancement and Image Analysis algorithms.

In this paper, we will present the implementation of a generic wavelet filter by iteratively using a dynamic-length 1-D filter. This filter can be used to perform a 2-D filtering by iterating the filtering process of the 1-D filter twice, one in the row direction and the other in the column direction. This technique will reduce the number of computations or operations performed on the image to produce faster results.

The image/data to be filtered is stored on the onboard memory. The processing kernel coefficients is computed by the software and sent to the hardware. These coefficients are used to generate a 1-D filter which cane be used iteratively to achieve higher dimension filtering. We have implemented Daubechy-2 by using a 1x4 kernel to compute 1-D filtering of the image and then feeding the filtered image back to a 4x1 filter which has the same coefficients. First we perform image filtering as rows which results in the 1-D transform of the image then the resulting image is again passed as columns through the same filter which is equivalent to a 2-D transform of the original image.

Our experiments show the superiority of Hybrid Reconfigurable Computers over pure software solutions in terms of speed/throughput. At the same time, these computers provide the flexibility of using dynamic-length filters in contrast to the conventional ASIC's implementation of fixed length filters.