

Software/Hardware Reconfigurable Network Processor for Space Networks

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In the paper we present a reconfigurable telecommunications/navigation network processor, we call the NavaTyrr, suitable for space-based applications. The prototype system is currently operating in a laboratory environment at JPL. The primary aspects of the design paradigm are presented here as well the specific implementation of the reconfigurable network processor currently operating in the lab.

The first element of the design paradigm is the use of a software reconfigurable processing platform, integrating both Field Programmable Gate Array (FPGA) hardware and a high-performance RISC processor. The other elements of the design paradigm are the methodologies for infusing signal processing and network processing algorithms and architectures common to space navigation and telecommunications networks into the implementation platform, at virtually anytime during the operational life of the platform. The development methodologies we have adopted leverage off of numerous high-level software/hardware development tools. These tools were chosen to accelerate design time not only for prototype development but even more importantly for subsequent improvements or even radical changes during the operational life of the system. In other words, implementation changes after a system has been launched and integrated into a specific science or technology mission.

Any hardware intended for space use must be tolerant of radiation effects. We provide an overview of FPGA scrubbing techniques developed to minimize the effects of radiation on a Xilinx FPGA. An important aspect of our software/hardware reconfigurable platform is partial reconfiguration. We envision having multiple transceiver channels in our FPGA. Partial reconfiguration will allow us, for example, to reconfigure, deactivate, or activate one or more receiver channels in the FPGA while keeping other communications channels running in the FPGA without interruption.

We present the implementation and performance results of a specific software radio and network processing system which together implement the bottom three layers of the OSI network model. This system is currently operating in the lab at JPL and is part of an ongoing program to develop improved technology for Mars network applications as well as a host of other space mission including formation-flying missions where multiple nodes will exist in a communications network. Specifically the NavaTyrr is being integrated in the CCNT instrument on Space Technology-5 spacecraft and the NEIGE instrument to be flown aboard CNES's Premier orbiter. The network processor demonstrated in the laboratory incorporates the

following: a reconfigurable BPSK radio implemented in hardware and software (layer 1), Proximity-one protocol implemented in hardware and software (layers 2 and 3), and TCP-IP Ethernet bridge implemented in software.

The reconfigurable BPSK radio can receive and transmit data rates between 1 kbps and 4 Mbps, using either NRZ or Manchester (Bi-phase L) coding schemes. The carrier frequency is yet another programmable parameter. The carrier phase synchronization and symbol synchronization loops in the receiver have programmable on-the-fly loop filter bandwidths. Software not only controls these various hardware parameters mentioned, but also performs real time tasks crucial to the receiver functionality. This includes open loop carrier frequency acquisition, lock detection, power estimation of carrier, uploading/downloading data from software to hardware and visa versa, and implementation of the digital automatic gain control (AGC) loop as well as other functions.

The Proximity-1 space link protocol specifies the Physical Layer, the Medium Access control layer, and is the Data Link Layer protocol for space communications. Proximity-1 is implemented in both software and hardware of the NavaTyrr, with the majority of its functionality implemented in the RISC processor. As part of the Data Link Layer, Proximity-1 acts as software controller of the hardware, turning on/off parts of the transceiver when necessary, changing data rates, managing the data, etc.

Finally, due to the generic methods and processing hardware of the reconfigurable network processor, we present the system as a suitable platform for implementing a wide variety of applications. These include radiation tolerant hybrid hardware/software processing required for science instrument data processing and rapid prototyping of communications, signal processing, and network algorithms.