

# The Multiversion Design Technology of an Onboard Fault-Tolerant FPGA Devices

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**Introduction.** The growth of complexity of functions carried out by digital devices (DD) of onboard control and information processing systems (CPS) is accompanied by increase of the reliability requirements, size-mass and power consumption restrictions. The search of compromise at FPGA DD (FDD) designing demands development of reservation methods or harmonious combination of known methods (taking into account the features of FPGA element failures) and means of fault-tolerant structures integration [1,2]. Besides the possible failure preconditions (due to imperfection of specifications, mathematical and graphic models of designed DD) and reliability of means used for FPGA designing and testing should be taken into account. It is especially important for unmanned or partially maintained real-time CPSs for aerospace and other critical applications.

The *purpose of report* is the presentation of design technology of fault-tolerant FDDs (FTFDDs). These devices should be tolerant to failures of on-chip and off-chip elements, design process and tool defects.

**General characteristic of technology.** The offered technology is based on results of decision of the following problems.

1. Formation of database of typical FTFDD structures. The various methods and means of on-chip and off-chip reservation, control and reconfiguration of FPGA channels are used in these structures.

2. Expansion (addition) of this database by use of a multiversity principle for design of reserved channels (on-chip channels and FDD channels as a whole).

3. Development of mathematical (combinatorial-probabilistic) and simulation models of reliability assessment of fault-tolerant structures which are included in extended database. These models should take into account failure flows of various FDD elements, design and tool defects, features of real-time CPS operation, and estimate other FTFDD characteristics (size-mass, power consumption, etc).

4. Choice of optimum FTFDD structure by the use of criterion:

) minimal cost - required reliability - size-mass and power consumption characteristics restrictions;

b) maximal reliability - size-mass and power consumption characteristics restrictions.

**Formation of the FTFDD database.** The database is developed by use of the following classification attributes:

a) type of redundancy (structural, temporary, version), Red;

b) checking means (built-in or external, i.e. on-chip or off-chip, functional or test checking), Ch;

c) reconfiguration means (built-in or external, standard or special), Rec;

d) level of reservation (on-chip or off-chip), L;

e) method of reservation, Rez.

The following methods of reservation are used: duplication, majorization. (non-adaptive or adaptive), reservation by replacement, sliding reservation. The received set of FTFDD structures  $MS = \{ S_j, j = 1, \dots, N \}$  forms a hierarchical tree. Further database of FTFDD structures is extended according to different kinds of version redundancy (diversity). This redundancy is based on use of:

) various initial models;

b) various design and testing techniques and tools;

c) various combinations of the versions of FDD functions performance on on-chip and off-chip levels and various location of scheme elements into FPGA;

d) FPGA of various manufacturers for design of FTFDD reserved channels.

The formation and choice of version redundancy variants (attribute V) is carried out by use of special techniques [3, 4]. The developed database contains several hundreds of formalized FTFDD structures  $S_j$  (Red, Rez, Ch, Rec, L, V) constituting the set MS.

**Models of FTFDD reliability assessment.** The following modes of failures are taken into account for development of FTFDD reliability models:

) internal structure FPGA (on-chip) failures,  $F_i$ ;

b) failures of the off-chip control, reservation and reconfiguration means,  $F_o$ ;

c) failures of points of FPGA and other FDD elements,  $F_c$ ;

d) faults and failures caused by design defects and other types of defects (imperfection of the specifications, models, tools),  $F_d$ .

The reliability estimation is made by use of combinatorial-probabilistic models based on consideration of events caused by failures from set  $F = \{ F_i, F_o, F_c, F_d \}$ . Besides the system of parallel simulation (imitating) modeling of structures  $S_j \in MS$  is developed for more accurate and detailed FTFDD assessment. This system allows to compare their

behavior on sets of situations differed by temporary and event characteristics taking into account quality of element manufacturing, influence of environmental conditions on changes of FPGA parameters, distribution laws for  $F_j \in MF$ .

**Results of researches.** The analytical models of reliability of FTFDD structures are developed. These models permit to calculate the probabilities of non-failure operation of one reserved channel,  $r_{rc}$  and FTFDD structure as a whole,  $r$ . The exponential and other laws of distribution of time to different mode failures are accepted according with results of the experimental data analysis [5] and other factors.

The analysis of reliability of FTFDD structures with off-chip and on-chip duplication allows to conclude that these structures have reliability smaller, than  $r_{rc}$  for all values of parameters (failure rate,  $\lambda$ , reliability of checking,  $D_c$ , number of the digits,  $n$ , and time,  $t$ ). It is caused by the fact that reliability of external elements (in relation to FPGA) is less than reliability of a chip, and also by great number of soldering connections. The influence of these two factors grows with increase of number of the digits in DD. Among structures with external duplication and on-chip majorization the structure with minimal quantity of external elements has reliability advantage. The several results of research of such structure are given in the next table:

Reliability of checking, $D_c$	Number of the digits, $n$	Operating time, $t$	Result of comparison
1	1, 4, 8, 16, 32	1 h, 1 m, 1 year, 5 years	< $r_{rc}$
0,9	1, 4, 8, 16, 32	1 h, 1 m, 1 year, 5 years	> $r_{rc}$ < $r_{rc}$
0,8	1, 4, 8, 16, 32	1 h, 1 m, 1 year, 5 years	> $r_{rc}$ < $r_{rc}$

The structure with off-chip duplication and on-chip majorization without external elements has the best parameters of reliability in all range of researched values. Application of FTFDD structures with on-chip duplication and off-chip majorization is expedient if  $n=1$ . The structures with on-chip duplication and off-chip majorization have higher reliability comparing with structures without off-chip elements (if  $D_c < 0,9$  and  $n = 1$ ). These results are corrected for multiversion FTFDD structures considering failure rate caused by design defects [1].

**Conclusion. Practical results.** The elements of multiversity technology are realized by use of standard tools (MAX + Plus II, FPGA Express, Actel DeskTOP). The given tools should be supplemented by a database of FTFDD structures and software for analytical and simulation modeling. It allows to provide multiversity in an estimation of reliability and to increase its accuracy [6]. The considered principles are the basis of automated system for the real-time FTFDD design (system SIROP).

Use of dynamic (real-time) reconfiguration is expedient for safety related CPSs with long duration of operation. It is realized by "modulation" of algorithms of FPGA programming by an information about detected faults. Thus the expenses caused by additional hardware-software tools and influence of their reliability on non-failure operation should be taken into account. Such dynamic reconfiguration (together with multiversity of structures and technology) provides an opportunity for controlled multistage FTFDD degradation and raises survivability in extreme conditions [7].

The principles of development of database, the technique of reliability analysis and choice of rational FTFDD structures were used in deicing system and system of air preparation of the plane N-70. Besides the offered technology is used at modeling of air conditioning system of the plane N-140.

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