

Update on Total Dose and Single Event Effects Testing of the Intel Pentium III (P3) and AMD K7 Microprocessors

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Abstract – To understand the radiation sensitivity and radiation response, Intel Pentium III and AMD K7 microprocessors were tested for total dose and single event effects. This paper represents an update to data presented at the 2001 Nuclear and Space Radiation Effects Conference.

I. Introduction

Many future NASA missions will require extensive on-board computation capability. The issue that this raises is the availability, cost and capability of currently available radiation hardened or radiation tolerant microprocessor systems. Radiation hardened computers systems are often costly and are actually two or three generations behind in computational capability. Additionally, the feasibility of a given mission may in fact require state-of-the-art (SOTA) capability.

To confront these issues, NASA has the Remote Exploration and Experimentation Project (REE). The goal of this project is to transfer commercial supercomputer technology into space using SOTA, low power, non-radiation-hardened, commercial-off-the-shelf (COTS) hardware and software to the maximum extent possible [1].

As part of this project, work was done to evaluate the radiation sensitivity and radiation response of the Intel Pentium III (P3) and AMD K7 microprocessors and their associated bridge chips. This paper will report of the total dose response (both proton and cobalt-60) and single event effects (proton and heavy ion) observed to date.

II. Test Methodology

Test System Description

The test system, described from a hardware perspective, has three levels: the system level, the motherboard level and the device under test (DUT). Figure 1 illustrates the overall test configuration.

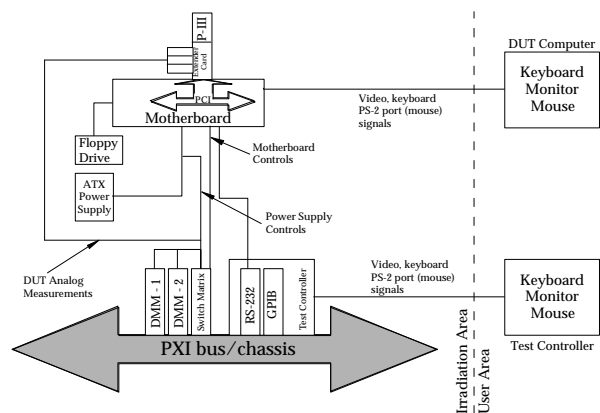


Figure 1. Block diagram showing the key features of the hardware setup for the testing.

The overall system consists of the necessary hardware to talk to and collect data from the motherboard and the DUT. It consists of item such as the PXI chassis that contains digital multimeters (DMM), the general-purpose interface bus (GPIB) and methods of talking to the motherboard. The motherboard is simply a COTS motherboard (a different one for the P3 and the K7). They have been modified, though, to supply key signals and allow for remote operation. Finally, the DUTs are also COTS parts modified in two manners. First, they are connected to the motherboard via an extender card that allows for the extraction of the various voltages and currents that are supplied to the microprocessor. Secondly, to allow for single event effect (SEE) testing, the DUT heatsink and fan assemblies removed and modifies so that the beams have a minimal material thickness to penetrate yet adequately remove the heat from the microprocessor.

The software used is based on the Pharlap embedded operating system. It is used by the DUT computer to execute the test code. The test code is written in C++ with Pharlap add-ins and Pharlap 386 assembly. Instructions beyond 386 are added with macros. The Pharlap add-ins enable remote debugging of the code through the serial ports.

The software executes with two or more threads. The main thread is executed upon booting the system from the disk. The main thread displays a menu and waits for another test to be selected. For all of the other tests, a second thread is launched to run the test software and the main thread goes into sleep. When the test completes the second thread is terminated. The main thread

displays a menu of all available tests to run as outlined below.

The test software sends a keep alive to the test hardware and the screen every second. If errors occur, the test software accumulates errors for one second and then dumps error codes to the test system and the screen.

TID Test Process

To do a complete characterization of the P3/K7 DUT for total dose effects would require numerous parametric measurements, too numerous to measure without test equipment beyond the scope of this project. This level of characterization is not necessary for the needs of this project. To this end, it will be sufficient to monitor: (1) the voltages and currents to the microprocessor (to monitor power draw), (2) instruction timing (to monitor the processor for timing critical operations), and (3) microprocessor functionality (the capability to run an operating system and test software the demonstrates functionality of all key processor features). Complete details of how these were performed will be included in the final paper.

Both P3 and K7 processors were evaluated for total dose response. This total dose response included exposure to protons at the Indiana University Cyclotron Facility (IUCF) and to Cobalt-60 at NASA Goddard Space Flight Center (GSFC). Testing has also been done using various microprocessor speeds and in an unbiased (all leads grounded) and biased (with software exercising the entire microprocessor) conditions.

Single Event Effects Test Process

The SEE test process must include methods to test for all aspects of single event effects (latchup, functional interrupts, upsets, etc.). As a number of these effects are sensitive to the software being run and may be sensitive to numerous other conditions, detailed control of the DUT is required. To this end, an extensive operating system would serve no purpose other than a software overhead that is uncontrollable. Therefore, the boot process was done into a minimal Pharlap operating system and a test executive was run that allowed testing sections of the DUT at a very low level.

The main part of the test flow is placing the DUT in a known operating state, waiting for something to happen and then dealing with it. Three general categories of events were expected: functional interrupts, system resets (radiation induced), and non-fatal errors (some error is produced but it does not immediately induce a functional interrupt or system reset. Once one of these conditions is seen and identified, the test process is to gain information about what exactly happened and to recover the DUT to a known state.

Testing has been done using various software routines to test sections of the microprocessor (e.g., registers, cache memory, floating-point unit, and MMX). Additionally, numerous processors speeds were tested including clocking-down processors in an attempt to investigate frequency dependent events.

III. Test Results

Total Dose

Intel P3 and AMD K7 parts were exposed to the total dose environment at the IUCF proton facility. The parts were exposed to protons in unbiased and biased states and exposed to proton doses ranging to approximately 100 krads(Si) with various increments. After each dose point, the all parts passed all functional tests and the monitored voltages and currents did not change. No parametric timing measurements were done in these tests. These tests are expected to be the most sensitive to dose. The parts, however, did not degrade in timing sufficiently to fail any of the functional tests that were performed.

Total dose testing using the Cobalt-60 source at GSFC is currently underway. Several P3 devices, in an unbiased condition, have been exposed to doses in excess of 400 krads(Si). They have shown little sign, if any, of degradation in either supply currents or timing and functionality testing. Biased testing of the P3 and K7 processors are either in progress or scheduled, with an expected completion data of the end of March

This total dose testing seems to indicate that this generation of P3 and K7 processors are TID hard to greater than 100 krad(Si). Based on the preliminary unbiased Cobalt testing, it is possible substantially higher than that.

Single Event Effects

Both P3 and K7 processors were evaluated for SEE response. This included exposure to protons at the IUCF and will include heavy ions at Texas A&M University Cyclotron (scheduled for mid March). Figures 2 through 4 show

a sampling of the proton data that has been collected and analyzed.

Figure 2 shows the SEFI cross section as a function of the cache state and the processor being tested. It is quite obvious from this figure that the cache represents the most sensitive region of the device and its operation causes the SEFI rate to increase by approximately an order of magnitude.

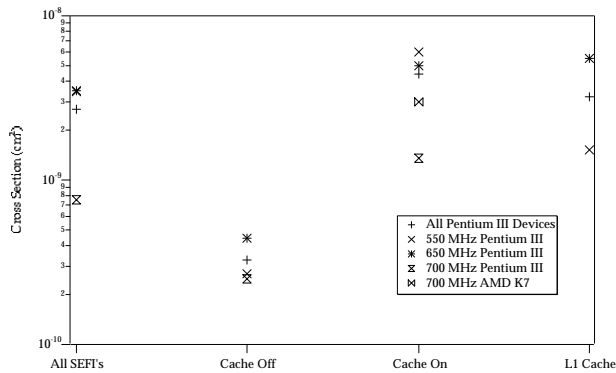


Figure 2. Plot showing the SEFI cross section as a function of the cache state during testing.

Figures 3 and 4 show the data from Figure 2 in a slightly different manner. Here the data is presented as a function of clock speed for both cases of cache on (Figure 3) and cache off (Figure 4). For at least the cache on state there appears to be a distinct difference in the cross section for the 466 and 700 MHz cases. These two cases are in fact the same processor that was clocked down for the 466 MHz case. There are many possibilities for this difference. For example this could represent true clock speed dependence or more likely a difference in the die layout or foundry process for the higher speed processor.

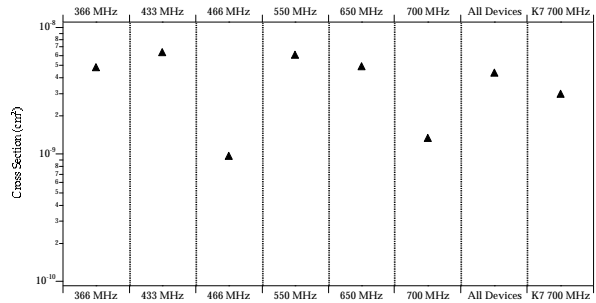


Figure 3. Plot showing the SEFI cross sections as a function of the device category for the case of "Cache On".

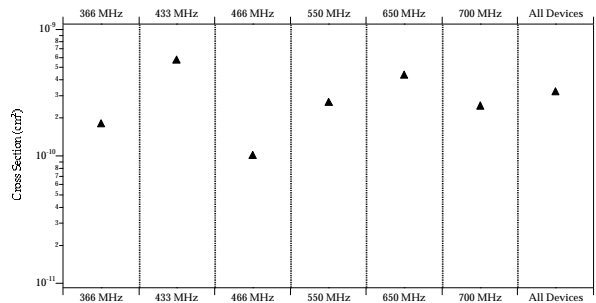


Figure 4. Plot showing the SEFI cross sections as a function of the device category for the case of "Cache Off".

Two proton tests have been performed that generated data on P3 devices, that ranged from 550 to 933 MHz, and K7 devices, that ranged from 600 to 1000 MHz. Testing was done that not only investigated the SEFI response, but also the latchup susceptibility and the upset sensitivity of the various components of the processors. This data, as well as the heavy ion data to be collected will be presented at the Data Workshop and the final paper.

IV. Conclusions

Extensive data has been collected on the total dose and single event response of the Intel Pentium III and the AMD K7 microprocessors. The data indicates that there is a high tolerance to total dose and there is no susceptibility to latchup from protons. Single event upsets and functional interrupts are present. However, if running with the caches disabled is an option and with mitigation in place, these events may be controllable to allow for operation in the space environment.

V. References

1. J. Beahan, L. Edmonds, R.D. Ferraro, A. Johnston, D.S. Katz, and R.R. Some, "Detailed Radiation Fault Modeling of the Remote Exploration and Experimentation (REE) First Generation Testbed Architecture", unpublished.