

Heavy ion irradiation of SRAM-based FPGA's

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In high radiation environments the use of rad-hard components is necessary but now the use of commercial devices is becoming more and more convenient because of several reasons. COTS Field Programmable Gate Arrays (FPGA) and industrial electronics strictly follow the rapid evolution of CMOS technology, featuring ever increasing densities and speeds at decreasing costs. The parallel evolution of Electronic Design Automation (EDA) tools and Intellectual Property (IP) industry enables a System on A Chip (SOC) paradigm on high-density re-programmable devices and this in turn allows a brand new approach for system level design. The impact of radiation damage on the performance of COTS FPGA's has been addressed by several works [1-4] during the past years. Both total dose and SEU sensitivity of various FPGA families have been tested. However, to our knowledge, less (or even no) attention has been paid to evaluating the radiation effects on parts of one of the more widespread supplier, e. g., Altera devices. In this work we have investigated heavy ion damage of Altera Flex-type components, which are just commercial components without any radiation qualification.

Our Devices Under Test (DUTs) were EPF10K100 manufactured by Altera, based on static RAMs for configuration memory, combinational part (lookup tables), and embedded memory. This FPGA has roughly 100,000 equivalent gates. The heavy ions used throughout our experiments had LET values between 1.6 MeV·cm²/mg and 62 MeV·cm²/mg. The experimental setup has been developed to test the FPGA in a dynamic mode, that is, by exposing a DUT with a running circuit to an ion beam. While this approach seems a natural choice, it should be complemented by a static mode of operation, that is, by exposing a configured and ready-to-run DUT to an ion beam. This second mode of operation relies on the possibility of reading back the configuration memory of the FPGA to check for SEU's, but, unfortunately, this feature is not supported by the silicon vendor and has not been done. Four Shift-Registers (S-R) implemented in the FPGA – two of which designed with Triple Module Redundancy (TMR) – are operated at a clock frequency of 30 MHz and their outputs are compared two by two (i. e., one TMR S-R was compared with one non-TMR S-R) to check equivalence at each clock cycle. Schematic of this design is drawn in Fig. 1. When a Single Event Upset (SEU) corrupts one S-R, the corresponding output signal differs from the reference signal and the abnormal condition is immediately detected via a monitor circuit controlled by a LabView program and the condition is timestamped and logged. The S-R is then automatically re-loaded and the system is ready to detect another SEU the next TRIG signal. The frequency of TRIG signal was of 50 kHz. If the SEU affects the configuration memory and/or control circuitry, the system may improperly works, but it is not able to reset/restart automatically. This error type is classified as a Single Event Functional Interrupt (SEFI) where the only possible operation is to switch off the FPGA and re-load the entire configuration memory. A second test procedure has been based on the measurement of the number of times that the supply current reaches an upper limit of supply current $I_{cc}=800$ mA during a given irradiation time. These measurements have been done by using a power supply that promptly stops the supplied voltage when current reaches 800 mA. This power stopping avoids the destruction of FPGA circuitry when a Single Event Latch-up (SEL) happens.

Our irradiation experiments have shown that SEFI's usually happen long before any observable SEU in the flip-flops of the SRs. We could observe SEFI induced errors by noting that the four output signals progressively disappear during irradiation. When the first signal disappears we take it as the *first error* and when all signals have disappeared we record the *last error*. All SEFIs observed during the irradiation experiments did not induce any latchup and were recoverable by cycling off-on the power: this suggests that the origin of SEFI may be correlated with the configuration memory or with the lookup tables that implement combinational logic in the DUT. A SEU in a RAM cell (configuration or lookup bit) causes the design corruption and hence the SEFI. This turned out to be by far the dominant effect during exposure, if compared to detected SEUs in the shift registers flip-flops and this agrees with the measurements and results already available for Actel and Xilinx SRAM-based FPGA [1, 2]. The detected *last error* shows a cross section that is about 10 times lower than cross section of *first error*. Probably *last error* measurements imply the corruption of almost all the configuration memory. Device cross section for various ions and LETs is plotted in Fig. 2. The difference between *first* and *last error* cross section is constant and about one order of magnitude.

Figs. 3 and 4 show the supply current versus time during two different runs with the same device in the same experimental conditions. The sudden increase of current of Fig. 4 (at about 730 s) could also be explained by a Single Event Latch-up [1], but we suppose that this event is not a SEL because this sudden current increase happens exactly when last error is recorded. This supply current increasing has been monitored (second test procedure) and from the fluence needed to cause $I_{cc}=800$ mA the device cross section was calculated. The current increase might be due to progressive SEU-induced driver contentions (e.g. two inverters trying to impose different logic levels on the same output) which are potentially high current absorption modes, but after power off-on cycle, the supply current returns at the original values ($I_{cc}=250$ mA). The current increasing during irradiation is so correlated with the alteration of bits in the configuration memory. By supposing that when $I_{cc}=800$ mA the configuration memory is completely changed, the device cross section has been calculated per bit and compared with that obtained by dynamic test (*last error*) in Fig. 5. Results of *last error* method and current monitor method are quite similar, and this indicates that the failure mechanism at the basis of the two different measures is similar or even the same. While this might not be obvious at first sight, it is sufficient to notice that *last error* dynamic test data are almost totally based on SEFI errors which are strongly correlated with SRAM upsets and these come at the expense of current increases because they are believed to be mainly due to driver contention [1]. The data can be reasonably fitted by the Weibull formula: $DCS(LET)=DCS_{sat} (1 - \exp\{-[(LET-LET_0)/W]^s\})$ where $DCS_{sat}=3.1 \cdot 10^{-2}$ cm², $LET_0=0.1$ MeV cm²/mg, $W=32$ and $s=5$. Finally, results of Fig. 5 are in good accordance to what found by Fuller et al. for Xilinx Virtex FPGAs [2].

References

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- [2] E. Fuller et al., "Radiation Characterization, and SEU Mitigation, of the Virtex FPGA for Space-Based Reconfigurable Computing" presented at 2000 NSREC, Reno, Nevada, July 2000
- [3] M. Ohlsson et al., 1998 IEEE Radiation Effects Data Workshop Record, Newport Beach, California July 24, 1998, pp. 177-180.
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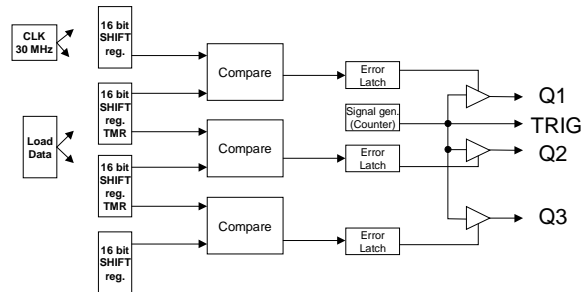


Fig. 1: Design implemented in the FPGA under test.

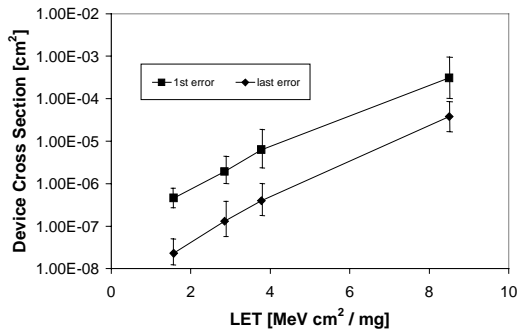


Fig. 2: Device cross section for low LET values. Bars are twice the standard deviation.

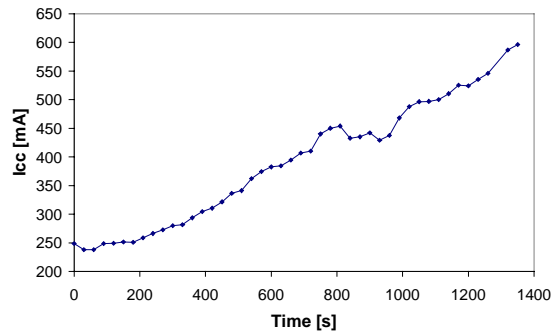


Fig. 3: I_{cc} current during irradiation with O ions ($LET=2.8$ MeV cm² / mg).

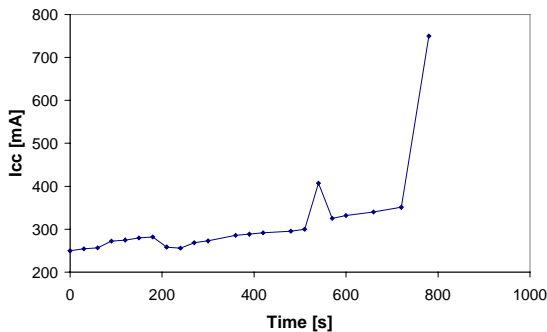


Fig. 4: I_{cc} current during irradiation with O ions ($LET=2.8$ MeV cm² / mg).

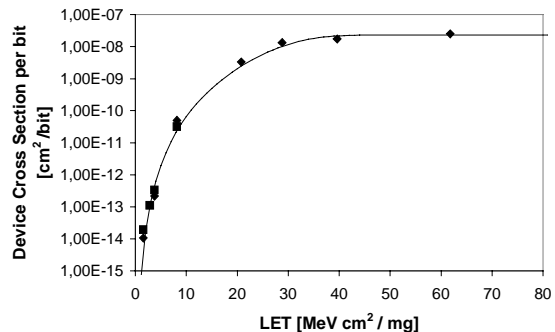


Fig. 5: Global device cross section per bit data. ♦ $I_{cc}=800$ mA, ■ last error.