Total Ionizing Dose Performance of SRAM-based FPGAs and supporting PROMS

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SRAM-based FPGA Advantages

- allows creation of standard multi-platform application modules (mission tailorable)
- supports re-configuration on-orbit or in space
- supports last minute design changes even after board build
- reduces design time
- reduces or eliminates tooling costs

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TID Testing Span

- low dose rates down to 0.015 rads(Si)/sec
  - simulated on-orbit dose rate
- high dose rates up to 50-300 rads(Si)/sec
  - Method 1019.5 compliant
- in-situ monitoring of key parameters
  - Icc, Tilo, other timing parameters
- utilized production final test programs
  - functionality, DC parametrics, AC timing

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Testing Methodology

- GammaCell at Lockheed-Martin Sunnyvale
  - available dose rate ~9.0 rads(Si)/sec
- Cobalt 60 source at McClellan
  - available dose rate 0.015 - 300 rads(Si)/sec
- all devices biased at nominal Vcc
- all tests utilized static bias
- annealing at room temperature and 100°C
- 1019 functional testing within one hour

Devices Tested for TID Response

- XQR4xxxXL - (XQR4062XL)
  - 3.3v 13,000 to 62,000 gates
- XQVRxxx - (XQVR300)
  - 2.5v 300,000 to 1,000,000 gates
- XCVxxxE - (XCV300E)
  - 1.8v 70,000 to 4,000,000 gates
- XQR1701L - (XQR1701L)
  - 3.3v 1,000,000 bit
- XQR18xx - (XQR1804)
  - 2.5v up to 4,000,000 bit

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XQR4062XL Process Description

- 0.35µM as-defined gate
- 65A gate oxide nominal
- isoplanar field - 7,500A nominal
- epitaxial substrate for SEL latch elimination
- engineered drain junctions
- dual diffused well isolation
- 3.3v operation and bias stress
- 3 layer metal with limited reflow & via fill
- fabricated at UMC Group

XQVR300 Process Description

- 0.25/0.35μM as-defined gate
- 45/65A gate oxide nominal
- shallow trench - 7,500A nominal
- epitaxial substrate for SEL latch elimination
- engineered drain junctions
- dual retro-grade well isolation
- 2.5v operation and bias stress
- 5 layer metal with CMP and via fill
- fabricated at UMC Group

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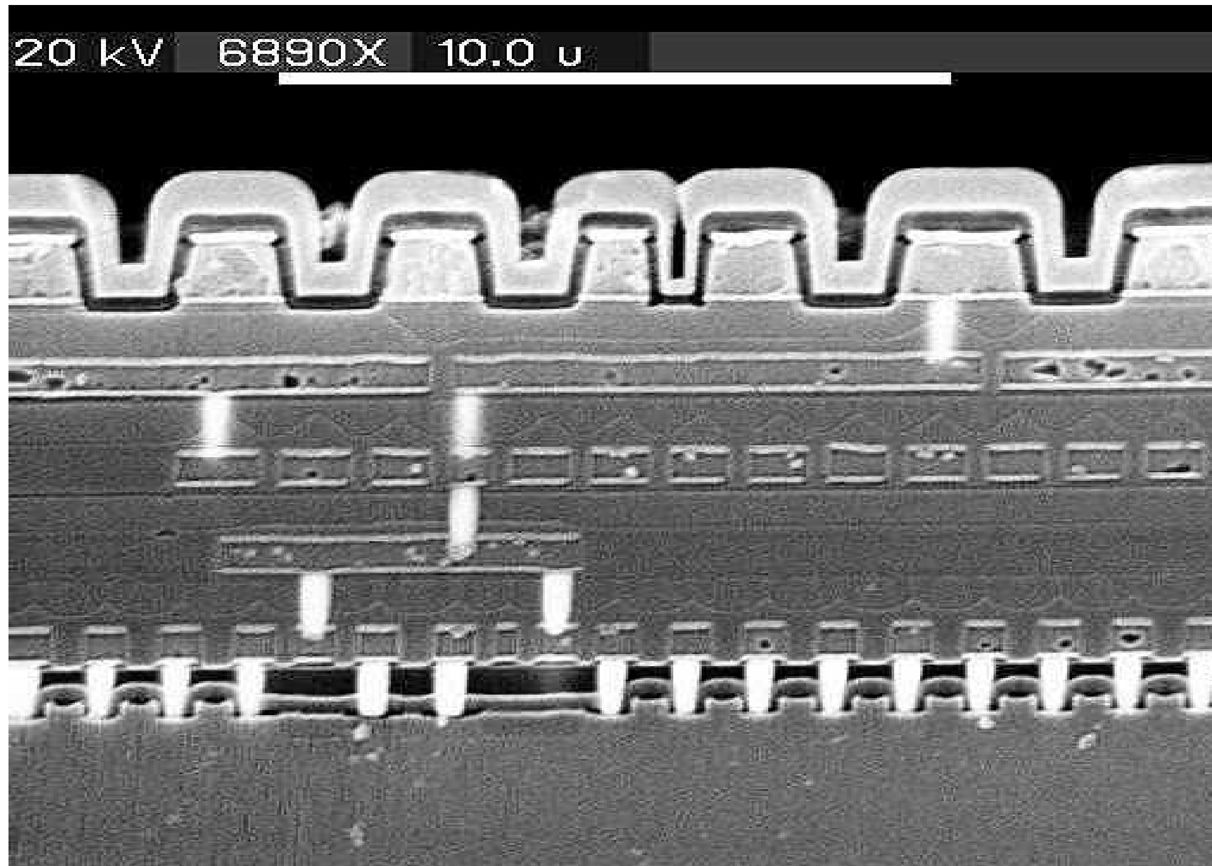
XQVR300 Topology



XCV300E Process Description

- 0.18/0.34μM as-defined gate
- 32/65A gate oxide nominal
- shallow trench - 6,500A nominal
- engineered drain junctions
- dual retro-grade well isolation
- 1.8v operation and bias stress
- 6 layer metal with CMP and via fill
- fabricated at UMC Group

XQR1701L Process Description

- 0.60µM defined gate
- 80A gate oxide nominal
- isoplanar field - 9,000A nominal
- epitaxial substrates for SEL latch elimination
- engineered drain junctions
- dual well isolation
- 3.3v operation and bias stress
- 3 layer metal with limited reflow
- fabricated at Seiko Epson

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XQR18xx Process Description

- 0.35µM defined gate
- 65A gate oxide nominal, flash
- shallow trench - 7,500A nominal
- epitaxial substrate for SEL latch elimination
- engineered drain junctions
- dual well isolation
- 2.5v operation and bias stress
- 2 layer metal with limited reflow
- fabricated at UMC Group

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TID Testing Results

- 0.35μM Technology
  - TID evaluation performed on XQR4036XL
  - device parametric shifts were negligible
  - field oxide leakage determined TID of 60krads
  - device fully functional at end of dose
  - 100°C anneal fully restored device
  - room temp anneal showed no rebound

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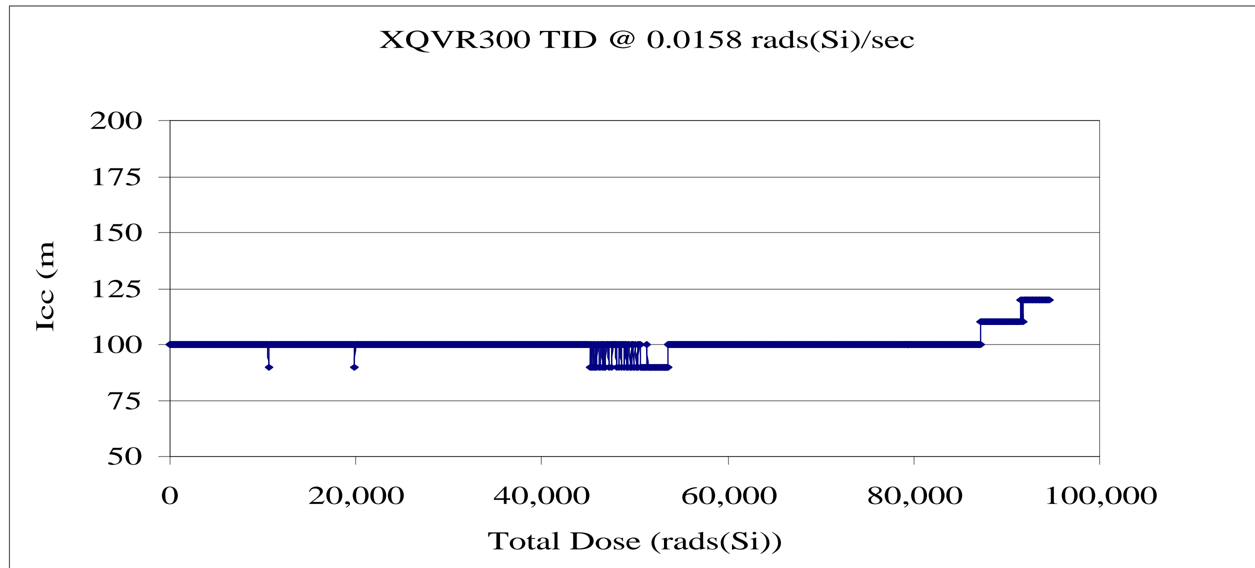
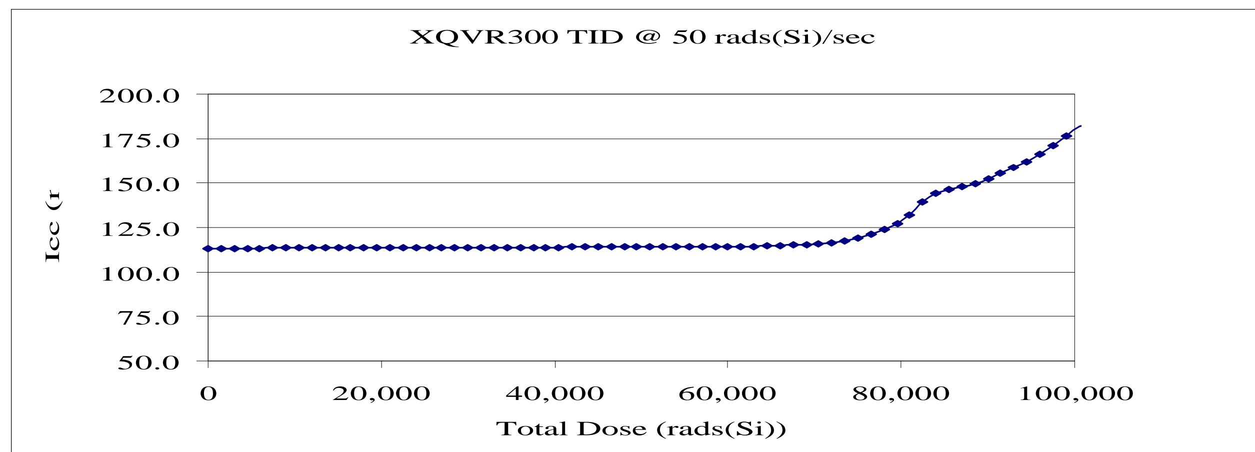
TID Testing Results

- 0.25µM Technology
  - TID evaluation performed on XQVR300
  - parametric shifts were negligible to 100krads
  - no leakage at trench isolation to 100krads
  - device fully functional at end of dose
  - slow increase in Tilo and other timings
  - 100°C anneal fully restored device
  - room temp anneal showed no rebound
  - no dose-rate effect over 4 orders of magnitude

Dose Rate Effects on 0.25µM Technology





TID Testing Results

- 0.18µM Technology
  - TID evaluation performed on XQVR300E
  - parametric shifts were negligible to >80krads
  - no leakage at trench isolation to >80krads
  - device fully functional at end of dose
  - slow increase in Tilo and other timings
  - 100°C anneal fully restored device
  - room temp anneal showed no rebound

Total Ionizing Dose Effect on 0.18µM Technology

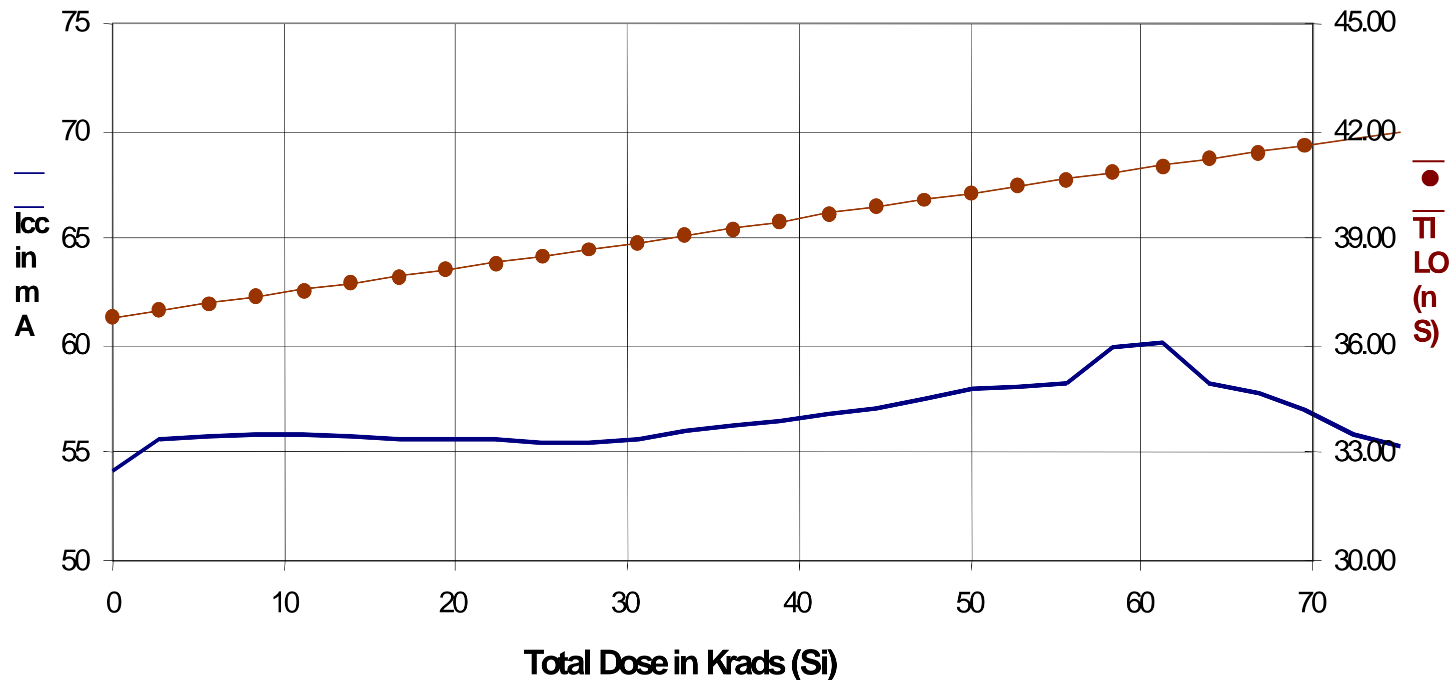


Figure 2. The radiation performance of a
0.18µM FPGA technology utilizing Trench Isolation

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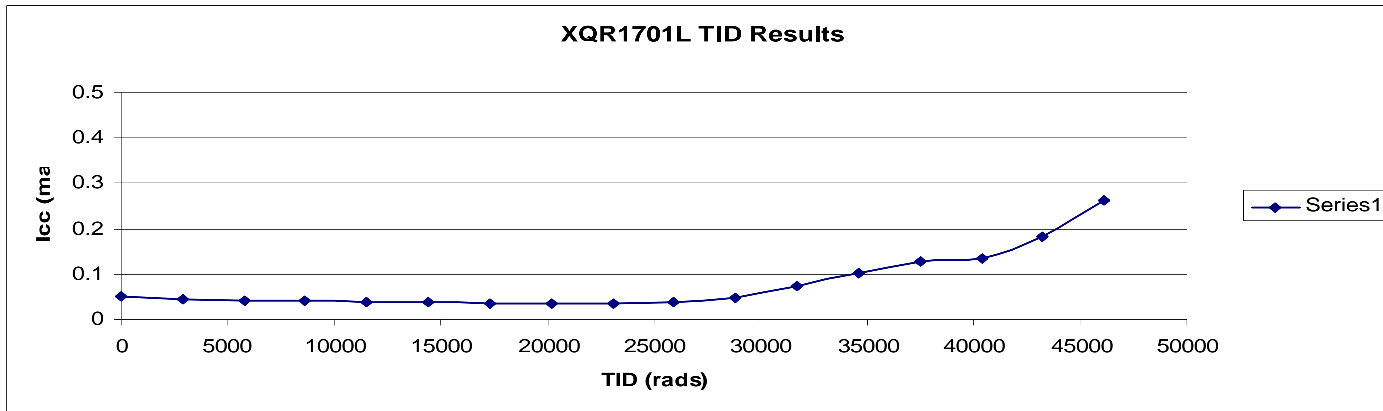
TID Testing Results

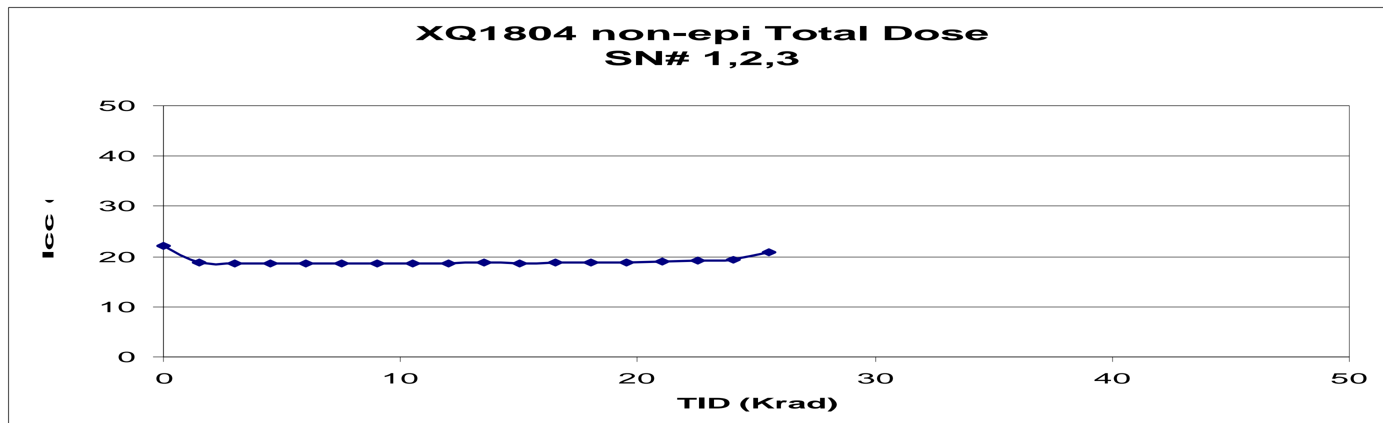
- 0.60µM OTP PROM Technology
  - TID evaluation performed on XQR1701L
  - device parametric shifts affected decoder speed
  - field oxide leakage determined TID of 60krads
  - device fully functional at end of dose
  - no data loss/gain as a result of TID
  - 100°C anneal fully restored device
  - room temp anneal showed no rebound

TID Testing Results

- 0.35µM ISP PROM Technology
  - TID evaluation performed on XQ1804 (XQR1804 will be tested in October, 2000)
  - device parametric shifts affected decoder function
  - no field oxide leakage to 60krads
  - device fully functional at 50krads
  - no data loss/gain in flash cells as a result of TID
  - 100°C anneal fully restored device
  - room temp anneal showed no rebound

PROM Response to TID





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Conclusion

- TID response of 3 families of FPGAs and two families of PROMS was measured
- results have been incorporated in data sheets of respective COTs devices
- no low dose enhancement was noted over 4 orders of magnitude of dose rate
- no rebound effects were seen

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