

Architecture of a Programmable Pattern Generator (PATGEN) ASIC for Space Applications

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Abstract

In this paper, we present the architecture for the Silicon on Insulator (SOI) Pattern Generation (PATGEN) focal plane array pattern generator Application Specific Integrated Circuit (ASIC). The PATGEN ASIC is a Focal Plane Array (FPA) or Charge Coupled Device (CCD) clock and control signal generation device for space applications. PATGEN is implemented in Ultra Thin Silicon (UTSi) technology for radiation tolerance; the device is extensible in both the number of output channels and the size of the patterns. The device is a digital pattern generation chip with two levels of looping. Patterns can be either single shot or continuous.

I. Introduction

The PATGEN avionics project is developing a detector clocking ASIC that will generate clock and control signals for CCDs or FPAs. The device can be in any space applications that require pattern or control signal generation. The PATGEN device is designed to have eight channels with eight fields per channel, (refer to Figure 1). Because each of the eight fields is 64 bits long, each channel can implement a pattern that is up to 512 bits long without any looping. The device also implements two levels of looping with up to 16K iterations each. The lowest level of looping is implemented as 16K iterations on each of eight 64-bit fields, and the second level of looping occurs at the sequencing structure. The sequencer has four groups in which each group is made up of a sequence of up to four fields. Each group allows for 16K iterations on each group sequence. See Figure 5 for a diagram of the looping structure. The pattern length can be reduced by half to permit high impedance outputs within the pattern.

Additional channels of patterns can be attained by adding devices in parallel. Adding more chips serially can attain longer patterns. Chips can be added serially and in parallel in a two dimensional manner to obtain more channels and longer patterns. In addition, the channels on a single device can be externally tied together to give longer pattern lengths.

The patterns are stored in a Programmable Read Only Memory (PROM) external to the PATGEN device. The PATGEN chip configures itself from the PROM on a power on reset. The PROM can be loaded with the configuration for several PATGEN devices. When

operating with multiple PATGEN chips, one chip is configured as the master, and this master chip drives the address lines to the PROM to configure all of the slave chips.

NASA Langley Research Center and Christopher Newport University (CNU) are partners on this project.

II. Radiation Requirements

Space applications are susceptible to Single Event Effects (SEE) causing intermittent failure, Total Ionizing Dose (TID) effects that shift transistor parameters causing failure over time and Latchup effects that can lead to catastrophic failure. Selection of an appropriate semiconductor process can reduce or eliminate these effects. For PATGEN, the Peregrine Semiconductor Silicon On Insulator (SOI) 0.5um UTSi fully depleted process was chosen. This process is available through the MOSIS service allowing for small quantity prototyping. Initial data from Peregrine (100Krad TID, <1e-09 errors/bit-day SEU, Latch-up immune) [3] appears more than adequate for many low earth orbit, geosynchronous and deep space missions [4]. The Peregrine process is fully depleted, Latchup immune, and free from kink effects [2].

Silicon On Insulator also has several advantages over bulk CMOS processes. One advantage is the reduction of parasitic devices. Because the transistors are built in an insulator and are isolated from one another rather than residing within wells, there are no parasitic devices created. Second, the losses associated with the parasitic devices are eliminated. This makes the devices faster and use less power than bulk devices. Third, the elimination of transistor wells means that the SOI devices will consume less area than their bulk counterparts. In general, SOI processes are considered comparable to the next generation of bulk CMOS. So, 0.5u SOI will be comparable to 0.35 bulk CMOS

III. Chip Architecture Overview

The PATGEN chip consists of the chip controller, eight identical channels, the Parity block and Bit Error block, shown in Figure 1.

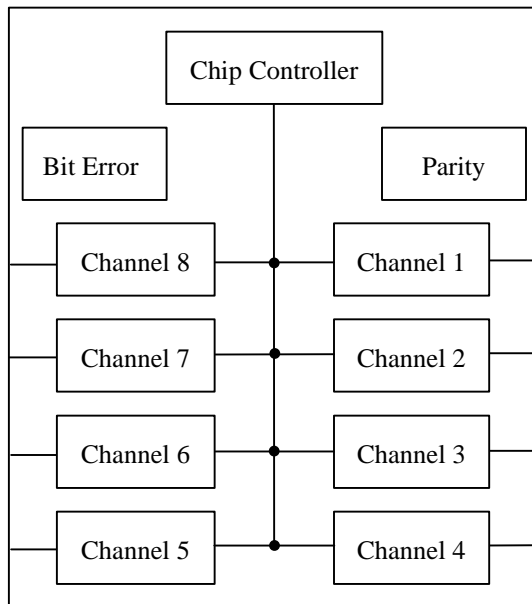


Figure 1 PATGEN top level

A. Chip Controller

The Chip controller consists of the chip enable logic, the address generator and the chip controller state machine. The purpose of the chip controller is to control the modes of operation, configuration of the chip, and synchronization. The chip controller uses the PEN (Pattern Enable) and PEND (Pattern End) signals to determine whether patterns are single shots or continuous. The mode of operation is determined by the chip controller state machine according to the levels present on the inputs M/S (Master/Slave), BIST (Built In Self Test), Begin_Init (Begin Initialization), the PStart (Pattern Start), and the PEN input.

B. Channel Block

The PATGEN channel block is comprised of: the channel controller block, the multiplexor and output enable block, the field length control block, eight identical field blocks, and the sequencer block. See the Figure 2 for the block diagram of a PATGEN Channel.

C. Channel Controller

The channel controller block is a small state machine made of two states (*reset* and *operating*), and the decode logic that controls the operation of the channel. In the operational state the channel controller sequences the control signals for loading and decrementing of all five types of counters that are in the channel. These counters are for the two levels of looping and the length of each field, the length of the group, and the length of the sequence.

D. Field Block

The field block is made up of a 64-bit cyclic shift register and a loop counter. The shift register is built of flip-flops and multiplexors. See Figure 3 for a diagram of the variable length cyclic shift register. The length control block enables the multiplexor that determines the length of the pattern, which allows the field size to be any length up to the 64-bit maximum. When enabled the field block shifts out the pattern, the multiplexors are all configured so the data shifted out is also shifted back in, reloading the shift register. This eliminates the need for a separate set of registers to hold the data.

The loop counter is a 14 bit down counter with reload register. This counter creates the first level of looping and allows for 16K iterations. Each field has its own loop counter.

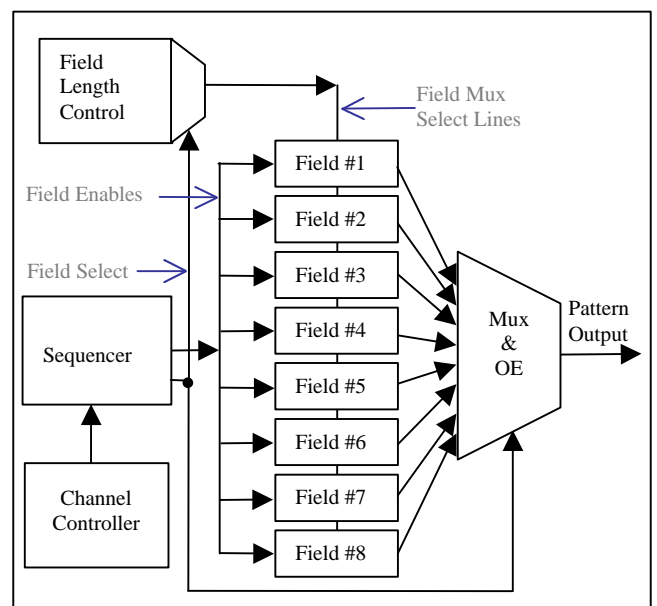


Figure 2 PATGEN Channel

E. Field Length Control

The field length control block consists of eight registers that hold the length of each of the fields. The registers are decoded to produce the enable bits for the field length multiplexors. The length decode process occurs when a field is selected by the sequencer block. When the sequencer selects a field to output its data it activates the field enable, selects the field for output on the output multiplexor, and selects the length register. Only the active field has its length decoded. By using the fields as sub-blocks of a pattern, the separate length registers allows the fields to vary in length so that arbitrary patterns can be built by using varying length fields with their own iteration counters.

F. Mux and Output Enable

The Mux and Output Enable block controls the output from the channel. The PATGEN chip outputs can operate in one of two output modes, either in a binary mode where the pattern outputs are either high or low, or in a mask mode where the outputs are tertiary and can take on high, low or a tri-state (high impedance state). In the binary mode the mask bit is cleared and the multiplexor uses outputs from the sequencer block to select from one of the eight fields to be output. If the mask bit is set then the four upper fields are used to set the pattern output to a high or low. The four lower fields determine when the pattern should be tri-stated. This allows the pattern to be high, low or tri-stated, but the pattern is only half as long (maximum length of up to four fields long).

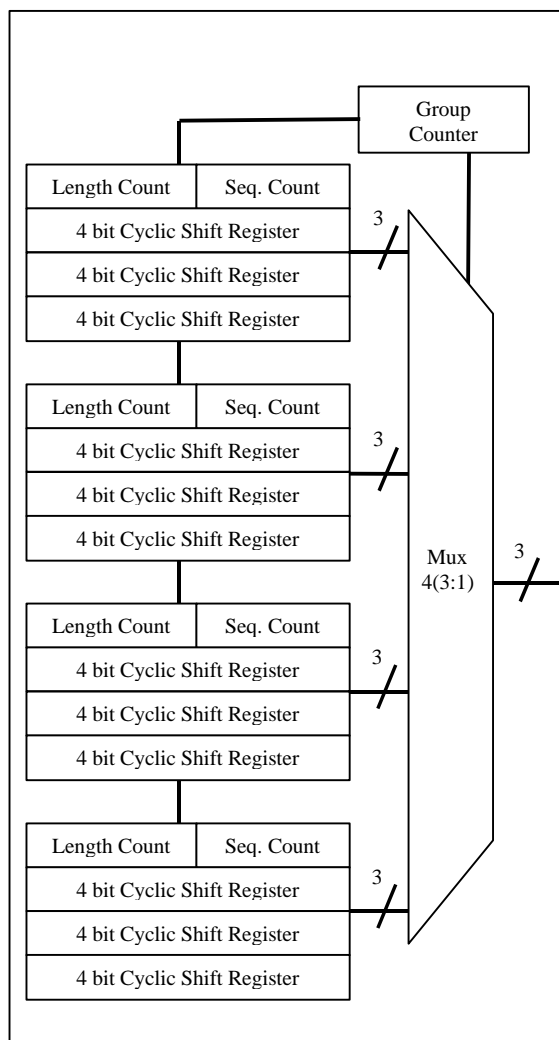


Figure 3 Sequencer Block Diagram

G. Sequencer Block

The sequencer block, shown in Figure 3, is comprised of four groups of sequencers. The groups are made up of small sequencers that each sequence up to four fields. Each

group has its own loop counter. This is the second level of looping and allows for up to 16K iterations. See Figure 5 for a block diagram of the looping structure. The group is made up of a set of three four-bit cyclic shift registers. The shift registers hold the values for the field that are to be selected. Since there are eight fields, there are three sets of shift registers. The output of the shift registers selects and enables the active fields, and it drives the select lines of the output multiplexor. The sequence length register controls the number of groups up to four, which can be chained together. This will allow up to 16 fields (four groups of four fields) to be sequenced. Since each channel only has eight fields, some fields must be used more than once for the maximum pattern length. See [1] for pattern examples and applications of the PATGEN chip. Since there are 64 bits per field, each with 16K iterations of looping, with four fields maximum per group, each group iterating 16K times and there are a maximum of four groups, the largest length of a single channel pattern is 256 Gbits.

IV. Auxiliary Functions

A. BIST mode

The BIST mode of operation disables the outputs and loads the chip from configuration data from the PROM. To enter the BIST mode, the BIST signal line is held high during a chip reset. To run BIST testing correctly, the channels need to be configured such that the output patterns satisfy even parity. The parity output then can be used as a BIST pass/fail indication. By properly choosing a pattern for the BIST mode, all bits within all of the fields as well as all of the counter bits can be checked for functionality.

B. Parity

The Parity block calculates the parity across the output of each of the channels. This bit is then output as the parity bit and can be used for error detection when transmitting the patterns as parallel data. During BIST mode the parity bit is used to check for errors during the self-test. In order for parity to work as the self-test error bit, the parity of the output channels must always be even while the self-test patterns are being generated.

C. Bit Error

The Bit error mode allows for SEU detection by performing a parity calculation on the data output from each channel. This is compared to the stored parity bits at the end of each of the patterns output. All of the separate channel parity bits are OR'd together to create a single Bit Error signal. If correct parity is observed, then the Bit_Error signal is low, and no SEUs have been detected. Otherwise, if an SEU has occurred, the Bit_Error signal is brought high, and the chip needs to be reset, which reset will reload the patterns and clear the problem.

V. Programmability

PATGEN is designed to have a flexible generic architecture that will permit easy programmability. The groups mentioned earlier are composed of up to four fields from the eight fields available. In addition, there can be up to four groups within a sequence. To illustrate how patterns are created, consider a sample pattern generated by a single group. Table 1 shows the bit patterns and the field numbers for four fields. The table also has the length of each field, the number of iterations for that field, labeled count, and the sequence number for the fields. For this example, the second level of looping in the sequencer is set up to loop three times on this group.

| FIELD NUMBER | PATTERN | LENGTH | COUNT | Seq. Number |
|--------------|----------|--------|-------|-------------|
| 5 | 111 | 3 | x1 | 2 |
| 7 | 11011011 | 8 | x2 | 1 |
| 2 | ZZZZ | 4 | x3 | 3 |
| 0 | 00000 | 5 | x1 | 0 |

Table 1 Channel Pattern Definition.

For this pattern definition, the output pattern would be:

```
00000 11011011 11011011 1111 ZZZZ ZZZZ ZZZZ
00000 11011011 11011011 1111 ZZZZ ZZZZ ZZZZ
00000 11011011 11011011 1111 ZZZZ ZZZZ ZZZZ.
```

The final pattern shown above can be set up to be single shot or to loop continuously. This example corresponds to using one group as shown in Figure 5. The red lines correspond to the iteration on the fields, the blue line corresponds to the three iterations performed on the group, and the green line corresponds to whether the pattern is continuous or single shot.

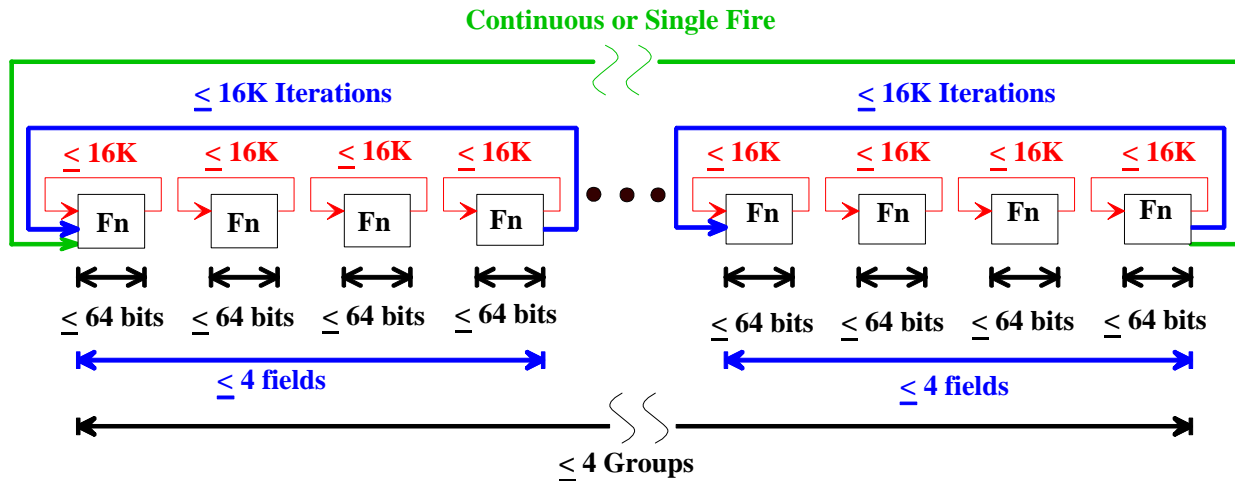


Figure 5 PATGEN Looping structure

VI. Software

To ease the burden of the FPA developer, PATGEN can be programmed graphically. A graphical editor, written in Java, allows the designer to enter the field patterns, enter the repetition counts, sequence field patterns together into groups, iterate on groups and chain groups together to describe complex waveform outputs. Once the patterns have been described in the PATGEN software, a PROM file can be exported. This file can be loaded into the boot PROM for the PATGEN chip(s) and is used to initialize the device(s) to the FPA developer's patterns prior to actual pattern generation. Figure 4 is a representative screen shot of the graphical entry tool developed for PATGEN.

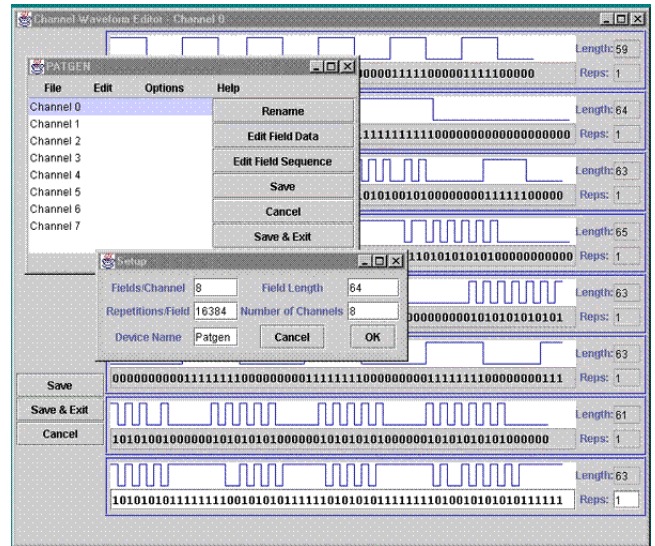


Figure 4 Graphical interface for pattern creation.

VII. Summary

The PATGEN device is a pattern generation chip that is extendable in the number of outputs and length of the patterns. Within the device, there are two levels of looping, each with 16K iterations. The patterns are made up of eight 64-bit fields, and can be continuous or single shot, and pattern lengths can vary from 512 bits to 256 Gbits in length depending on the amount of looping. The PATGEN programming software, a graphical entry tool for developing patterns, has been written, tested and documented. A prototype PATGEN chip has been fabricated using Peregrine's 0.5u SOS process through MOSIS. The prototype has two channels and the fields are only 32 bits wide instead of 64 bits. Device testing will begin in October of 2000.

VIII. References

- [1] R. F. Hodson, W. C. Wilson, C. D. Armstrong, Pattern Generation for Space Applications of Focal Plane Arrays, NASA Technical Memorandum
- [2] Colinge, Jean-Pierre, Silicon-On-Insulator Technology: Materials to VLSI, 2nd Edition, p127.
- [3] Lyons, G, Commercial SOS Technology for Radiation-Tolerant Space Applications, Radiation Effects Data Workshop, 1998. IEEE , 1998 , Page(s): 96 -99
- [4] Benedetto, J.M, Economy-Class Ion-defying ICs In Orbit. IEEE Spectrum Volume: 35 3, March 1998, Page(s): 36-41