

# Designing and Testing a Radiation Hardened 8051-like Micro-controller

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## *Abstract*

Micro-controllers operating under radiation condition (space and nuclear environment) can be affected by Single Events Upsets (SEUs). SEUs are responsible for transient changes in the information bits stored in integrated circuit. SEUs are a major concern in space environment, and have also been observed on ground levels as the result of interactions of neutrons in the atmosphere. The memory cells and registers included in microprocessors must be protected to avoid potential transient errors. This work presents a prototype of a hardened version of the 8051 micro-controller, entirely built with EPLDs. The developed processor is able to assure reliable operation in the presence of bit flips caused by radiation. The technique used in this work to detect and correct faults in the 8051 memory cells (registers or RAM cells) consists on codifying each memory element by Hamming code, and to perform the verification and correction of the stored word every time this memory point is accessed.

The radiation hardened version of the 8051 micro-controller was designed using the VHDL language. The choice of this micro-controller was based on the fact that it is widely used in space applications, and consequently, large amount of data about its behavior under radiation is available. Besides, its hardening makes possible the reuse and protection of all systems that are already running based on it.

The micro-controller VHDL description is divided into six main blocks. These units are the finite state machine, the control unit, the validation unit, the datapath and the RAM and ROM memories. The Finite State Machine (FSM) block generates the states and number of cycles for each instruction to guide the circuit operation. It has a very simple combinational logic and a set of flip-flops. The Control unit generates some control signals for the datapath, and it is basically composed of multiplexors. The Validation unit generates the microcode word for each instruction, and it is also basically composed of multiplexors. The Datapath includes an Arithmetic Logic Unit (ALU) and some registers.

Four structures in the 8051 VHDL description have been protected by Hamming Code: the Finite State Machine, the RAM memory, the Control unit and the Datapath. These blocks contain memory cells that can be affected by SEU radiation effects. The Validation unit is a completely combinational structure and in principle it is not subject to bit flips, requiring no protection schemes for it. The ROM block is also immune to these faults, since its content can not be modified.

The original version of the 8051 VHDL description has 106 stored bits used for internal registers and a 128-bytes internal RAM memory (1024 stored bits). The internal memory corresponds to 90% of the storage elements in the 8051. The control unit has one 8-bit register to store the instruction code, two store bits for the interruption state and one bit for the interrupt mechanism interface. The FSM unit has three 5-bit registers to store the current state, next state and the state of the micro-controller. The Datapath unit has several 8-bit

register, the accumulator (A), the program counter (PC), the stack pointer (SP) the two ALU inputs, the ALU output, the ROM address, the instruction code, the address register for the RAM and the input bus for the RAM.

The hardened 8051 version has 94% of the sensitive area protected: the internal RAM memory (90% of the sensitive area), some datapath registers (accumulator and program counter), the control unit registers and the FSM control registers (4%).

The hardened description was prototyped into three programmable logic devices customizable by EEPROM technology. PLDs customizable by EEPROM have been chosen to implement the first prototype of the fault tolerant 8051 micro-controller, since EEPROM elements are not so radiation sensitive as SRAM programmable memories cells used in FPGAs. In such way, device customization has less chance to be affected by the radiation environment and the fault tolerant 8051 implementation can be tested by itself.

There are some registers in the datapath that were not protected, since the used PLDs were not large enough to implement the datapath with all registers protected by hamming code. Moreover, the influence of a potential transient fault in these non protected registers must be analyzed. Testing these registers by fault injection is not possible when using the standard 8051 instruction set, because these registers are not accessible by the programmer. Aiming at verifying and testing the effects of transient faults in non-protected registers of this VHDL version, new instructions were developed and described, allowing access to internal register values. Using this approach it is possible to verify the consequences of transient faults in all registers and memory cells. The addition of these instructions increases the 8051 area around 10% but does not affect its performance. The trade-off between the final 8051 area and the area protected by hamming code can be analyzed using this method. This way, one can assure the amount of sensitive area that must be protected to reach the desired levels of immunity.

The robust 8051 board is being verified using a dedicated tester named THESIC developed by TIMA laboratory (France) to analyze the capabilities of this technique. The board will be tested under radiation by ground testing using THESIC environment. This board is also going to be test by fault inject. The faults will be injected in various storage elements such as accumulators, PC, SP, DPTR and RAM memory, by using the 8051 interruption signals instruction set. The potential transient faults in the other registers included in this hardened version of the 8051 can be accessed by these new instructions.

Preliminary results [COTA et al, LATW 2000] allow to predict that an 8051 robust version based on the hardening of internal RAM, datapath, control unit and finite machine registers by an error detection and correction strategy will tolerate almost 100% of the effects of transient bit flips. The first results in area evaluation show that the SEU immune processor is at least twice bigger when using PLDs. The presentation will describe in details the results obtained from the ground testing with the test chip.