Initial Single-Event Effects Testing and Mitigation in the Xilinx Virtex II-Pro FPGA

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Abstract

A consortium of industry and government partners has begun single-event effects testing on the Xilinx Virtex II-Pro FPGA for consideration in space applications. An initial static characterization of the FPGA fabric and some dynamic modes using input/output blocks has been done.

We present initial results for the Virtex II-Pro FPGA and compare to previous results obtained for the Virtex II family. In the early tests, the II-Pro device appears to have similar or improved radiation performance.

Definitions / Acronyms

FPGA: Field-Programmable Gate Array

IOB: Input/Output Block

DUT: Device Under Test

TMR: Triple-Modular-Redundancy *(strategy for mitigating effects of errors)*

SEU: Single Event Upset

SEFI: Single Event Functional Interruption

(SEU in control circuits that interrupt major device functions)

POR: Power-On-Reset *(POR SEFI causes device to reset and clear configuration)*

SelectMap: Parallel configuration interface

(SelectMap SEFI includes all configuration failures)

Latchup: A potentially destructive high-current mode caused by a charged particle

Static Test: Device irradiated without a running application

(readback configuration after test to find SEUs)

Dynamic Test: Device irradiated with a running design

Devices in the Virtex II family

Virtex II

- Dynamically configurable logic
- Dual-port BlockRAM
- Programmable I/O impedance
- 18x18-bit multiplier blocks
- Digital Clock Managers
- 300 MHz logic speed
- 150-nm, 8-layer Cu technology
- Total Dose > 200 krad

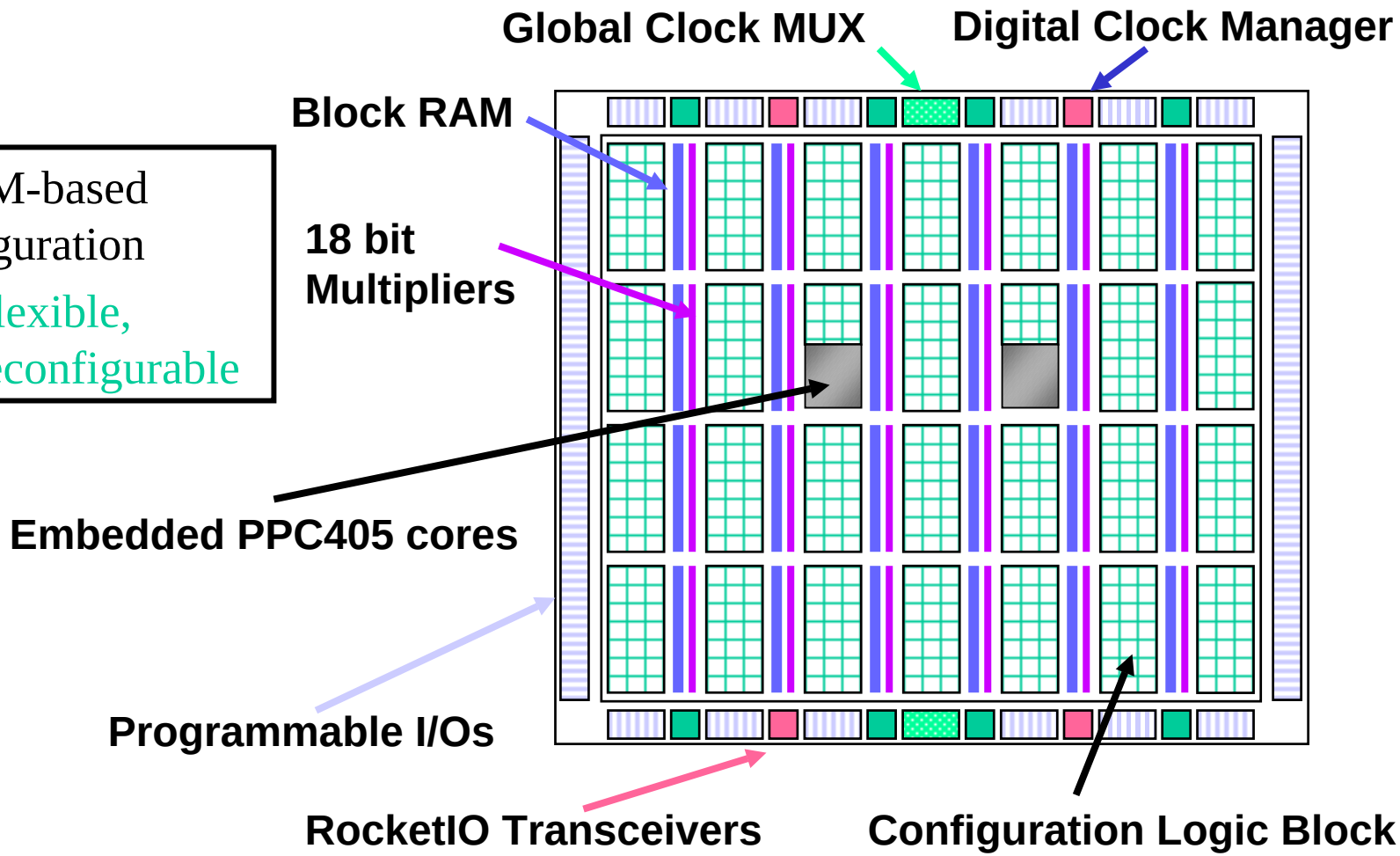
Virtex II-Pro

- 2 embedded PC405 cores
- RocketIO serial transceivers at 3.125 Gbps
- 130-nm, 9-layer Cu process
- 400 MHz logic speed
- TID > 300 krad

The Virtex II-Pro is faster, denser, and adds new features

Features of the Virtex-II PRO FPGA

- SRAM-based configuration
  - Flexible, reconfigurable



(drawing is a cartoon representation of the device major features)

Beam Summary

Texas A&M University Cyclotron Facility

Static Test ***(Range and LET values after passing thinned backside of device)***

Ion	LET (MeV-m^2/mg)	Range (um)	Notes
40 MeV/n Ne	1.27	1439	Angle and degrader
40 MeV/n Ar	4.22	407	Angle and degrader
25 MeV/n Kr	29.3	116	Also degrader
25 MeV/n Xe	58.4	70	0 degrees

Dynamic Test

Ion	LET (MeV-m^2/mg)	Range (um)	Notes
25 MeV/n Ne	2.01	582	Angle and degrader
25 MeV/n Ar	7.08	277	Angle and degrader
25 MeV/n Kr	29.3	116	Also degrader

Testing Objectives

- SEU sensitivity of V-II Pro “fabric”
  - Configuration and BlockRAM cells
- SEU sensitivity of Input/Output Blocks (IOBs)
  - In real design with and without using mitigation techniques
- Measure SEFI modes *(single event functional interruption)*
  - POR, SelectMap, IOB, and any new modes
- Compare results to Virtex-II data

Static Test Design

Measure upsets in configuration and BlockRAM cells

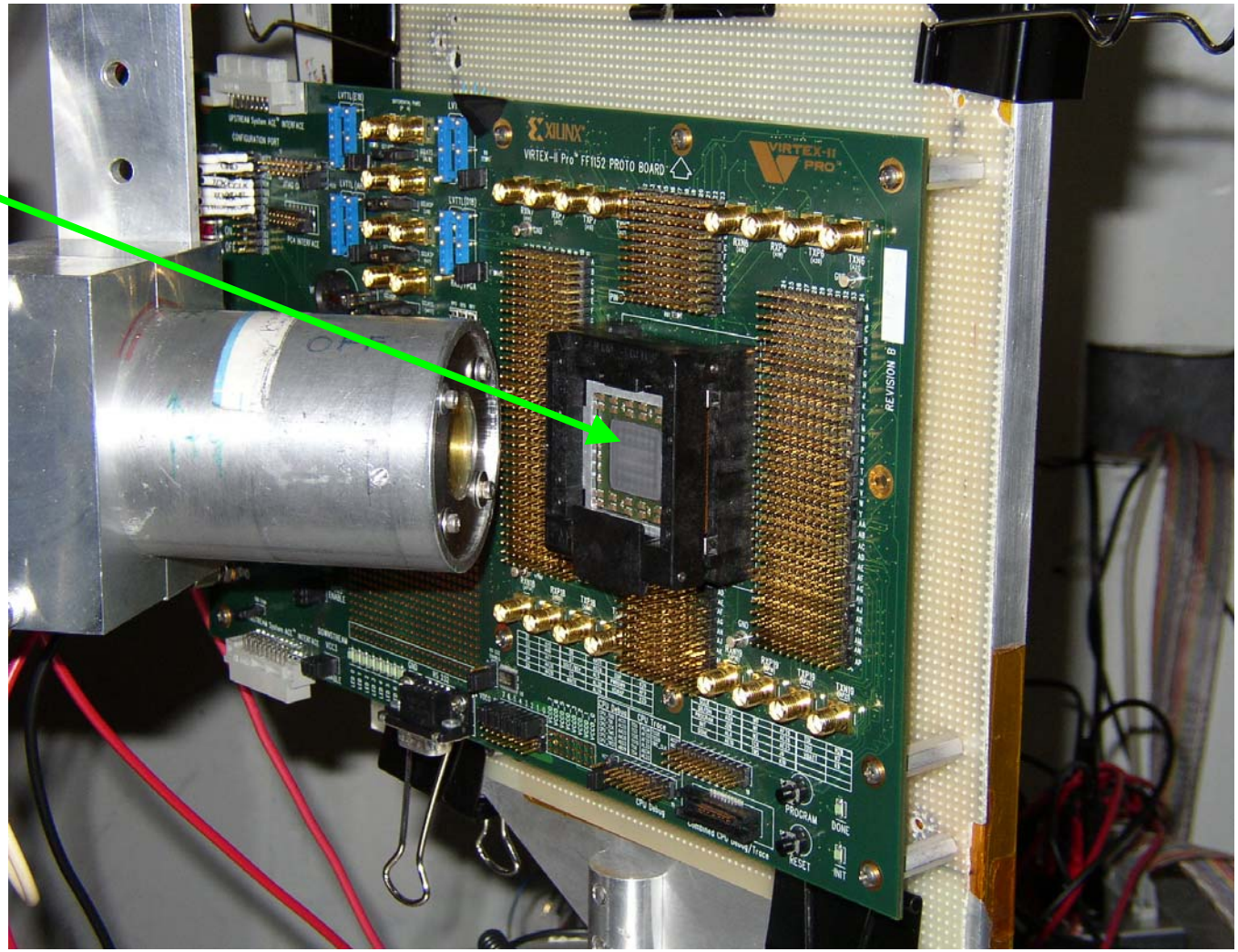
- FPGA is configured with a large user design
  - Fills configuration and BlockRAM with many 1's and 0's
- Irradiate part
- Read back configuration to check for static upsets

- Xilinx AFX Proto development board
  - XQR2VP40 Virtex-II Pro FPGA device

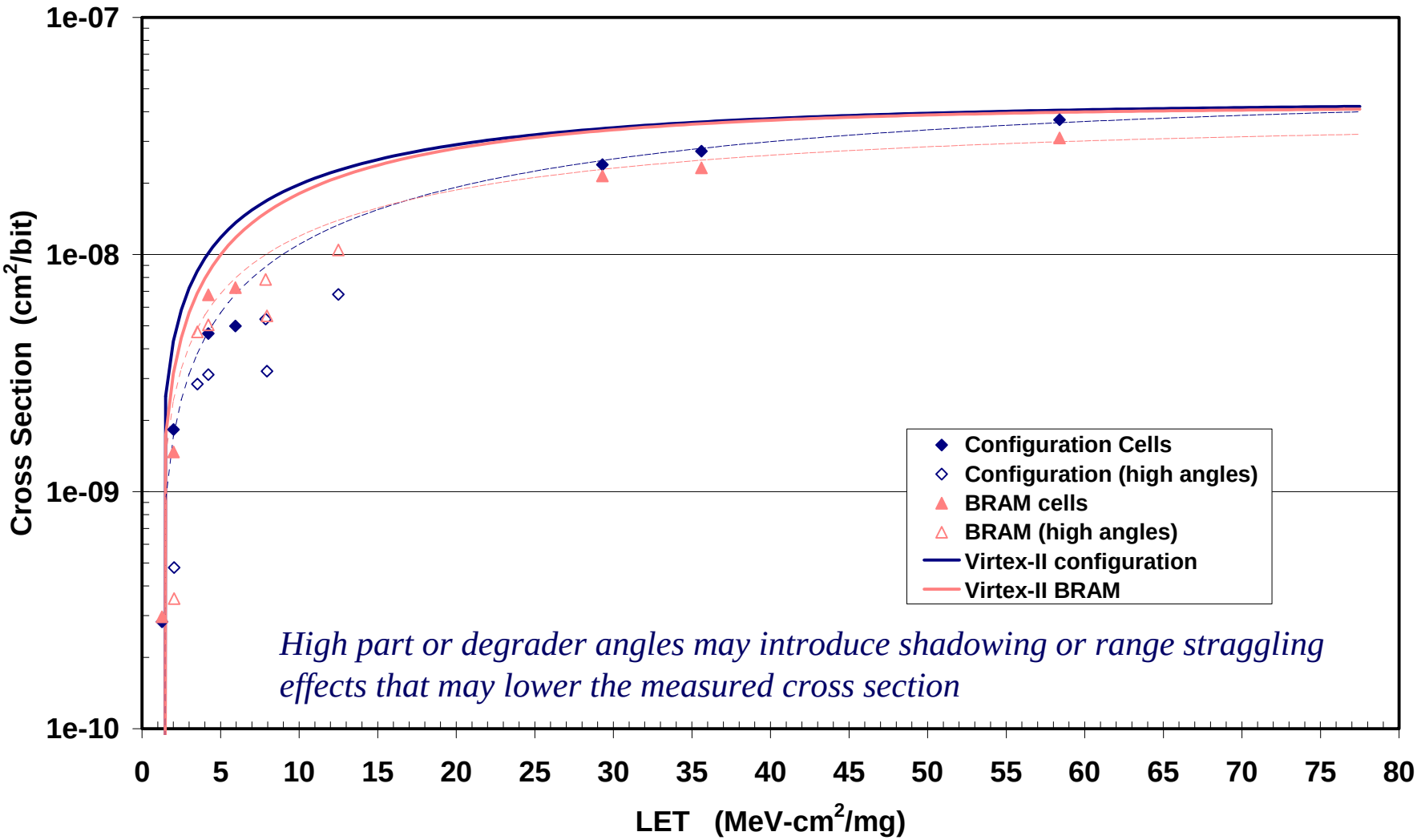
- Total configuration bits: 10,462,828
- Total BlockRAM bits: 3,538,944

Static Test Board Set-up

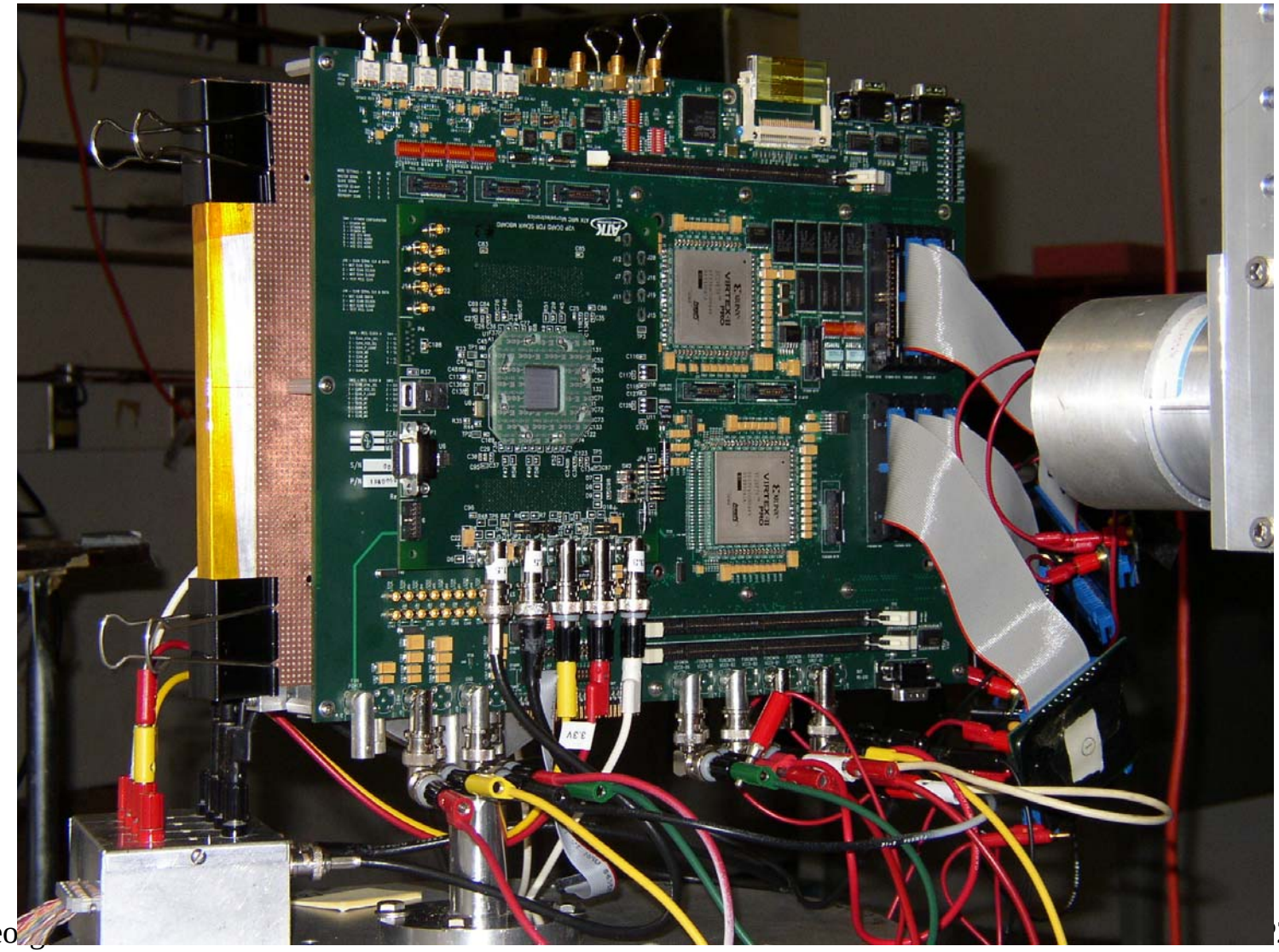
Test Device



Static Test Results



Dynamic Test Set-up

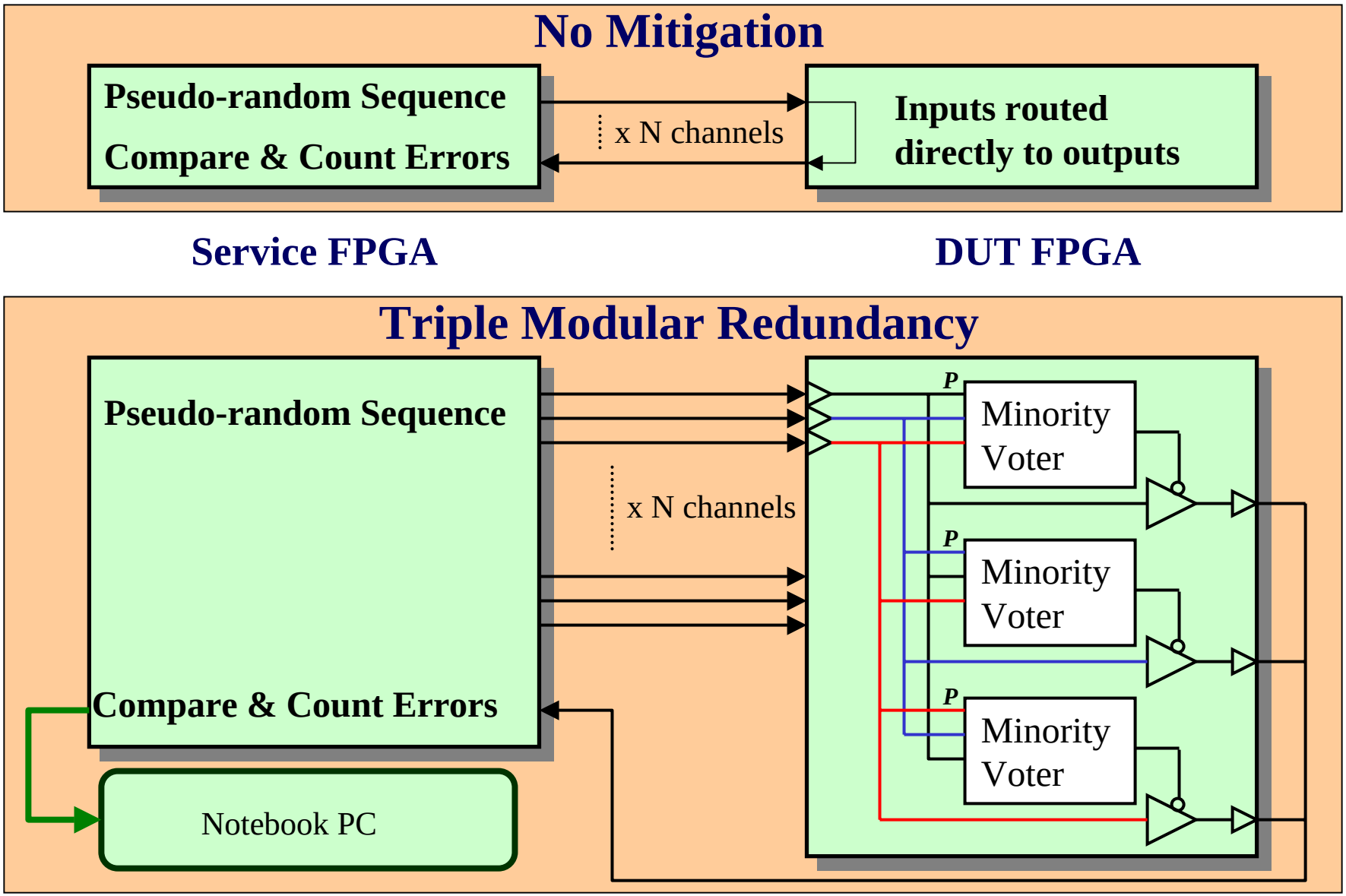


Dynamic Test Design

Measure SEFIs and IOB upsets with a running design

- Custom-built test board
  - 2 FPGAs: the “service” FPGA exercises and monitors the “DUT”
  - SEAKR Engineering, Inc.
  - XQR2VP40 Virtex-II Pro FPGA device
- Pseudo-random pattern is pushed through IOBs
  - Minimal routing inside the DUT
- A TMR mitigation strategy was also tested

IOB Mitigation



IOB Voltage Standards

We tested 2 different I/O voltage standards

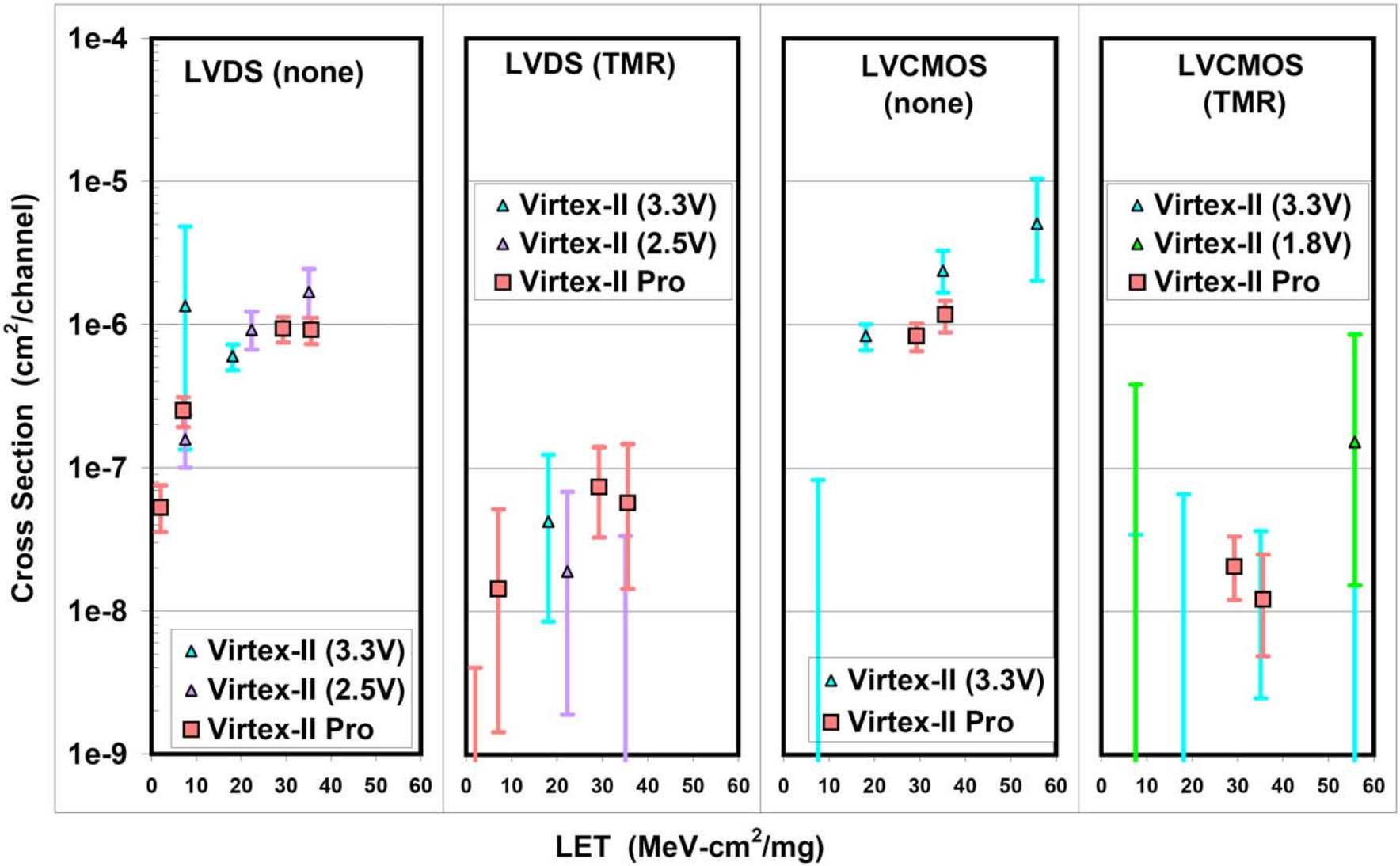
- LVCMOS 2.5V
  - No Mitigation: 93 separate IOB channels
  - Full TMR: 29 separate IOB channels
- LVDS 2.5V, 33 MHz
  - No Mitigation: 21 separate IOB channels
  - Full TMR: 7 separate IOB channels

SEFI and Latchup

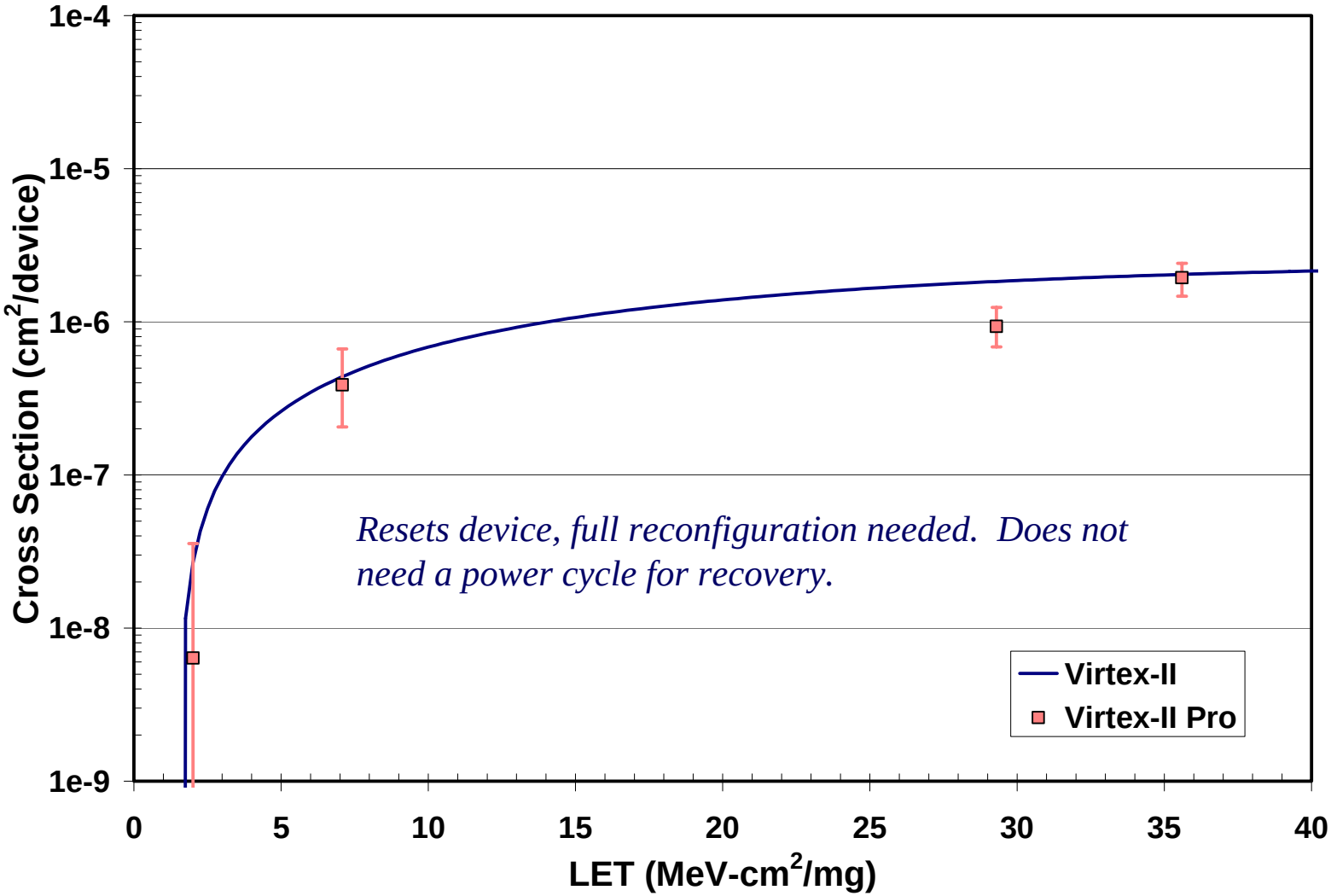
- POR and SelectMap SEFIs require reconfiguration.
  - Power cycling is NOT necessary.
- IOB “SEFI” disables all I/O channels.
  - Fixed by partial reconfiguration (scrubbing) alone.
  - Virtex-II Pro had “partial” mode with only some I/Os disabled
  - Power cycling is NOT necessary
- **NEW**: SEFI that requires a power cycle to recover
  - May be related to new features in Virtex-II Pro
    - i.e., configuration clock pin (CCLK) mode options
  - Needs further investigation

- No latchup seen at LET=35.6 with >3e7 ions/cm^2

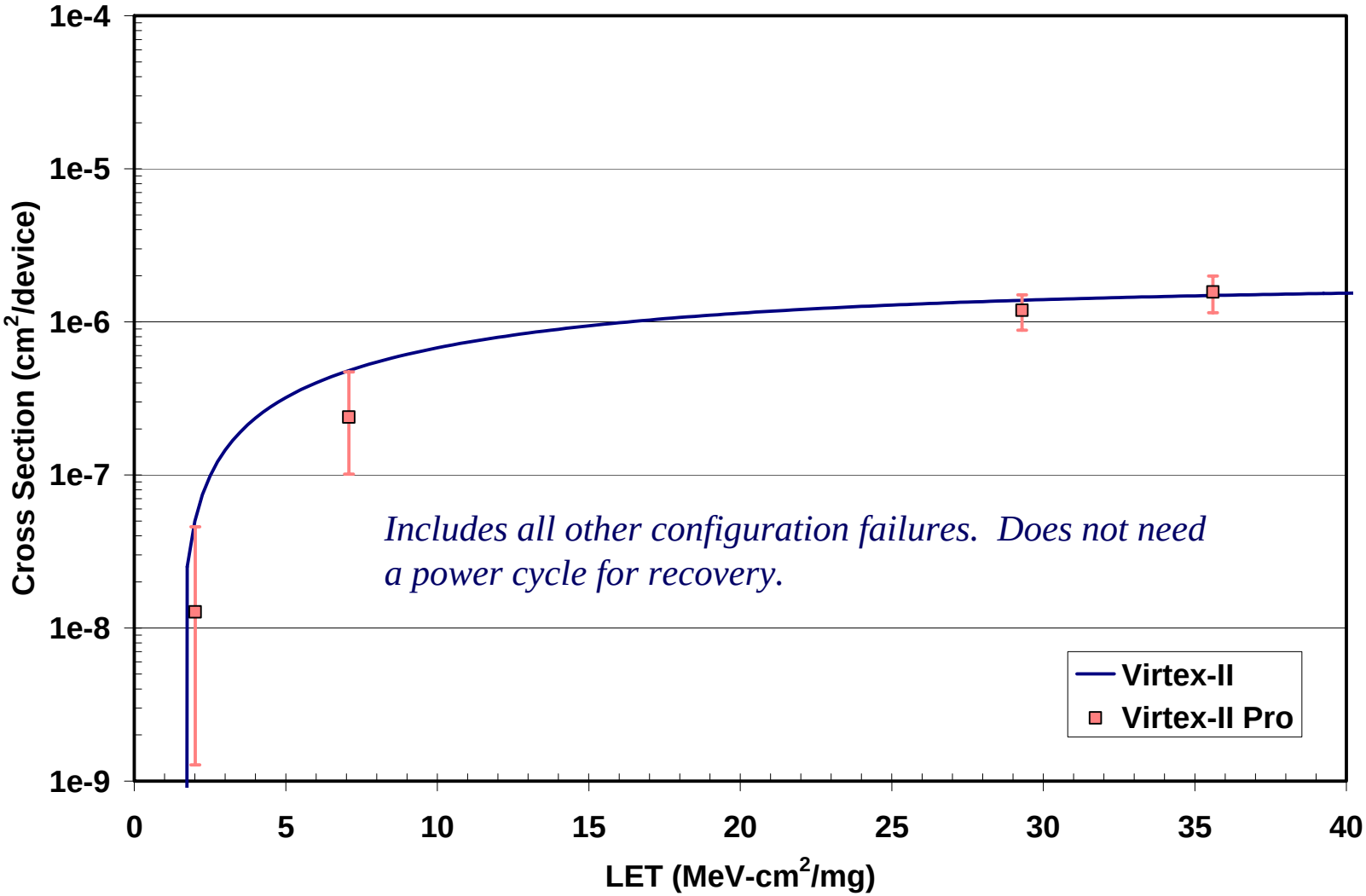
IOB Upsets


LVDS (none)
LVDS (TMR)
LVCMOS (none)
LVCMOS (TMR)
Virtex-II (3.3V)
Virtex-II (2.5V)
Virtex-II (1.8V)
Virtex-II Pro
Cross Section (cm²/channel)
1e-4
1e-5
1e-6
1e-7
1e-8
1e-9
0 10 20 30 40 50 60
LET (MeV-cm²/mg)

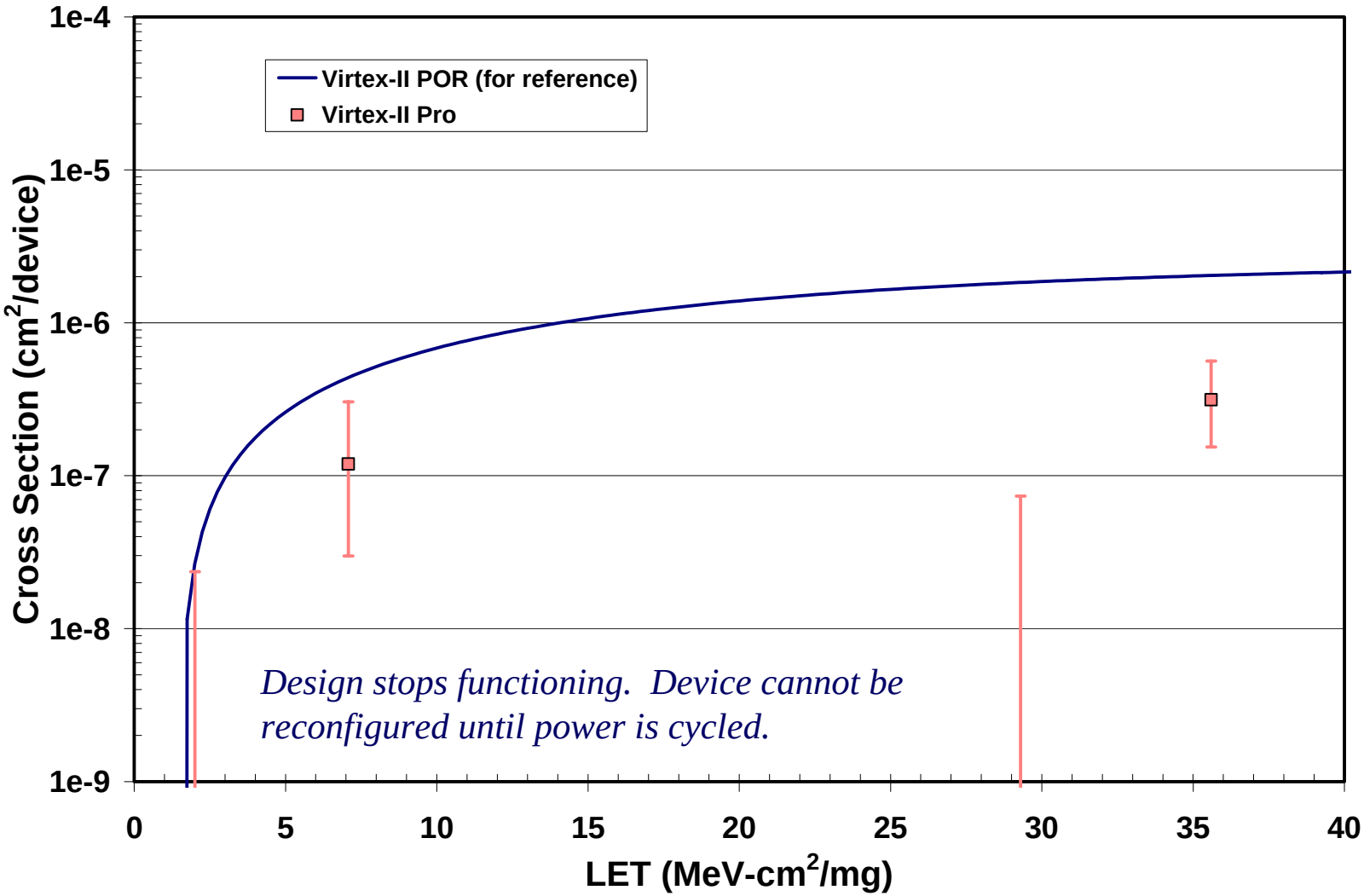
POR SEFI


1e-4
1e-5
1e-6
1e-7
1e-8
1e-9
Cross Section (cm2/device)
0
5
10
15
20
25
30
35
40
LET (MeV-cm2/mg)
Resets device, full reconfiguration needed. Does not need a power cycle for recovery.
Virtex-II
Virtex-II Pro

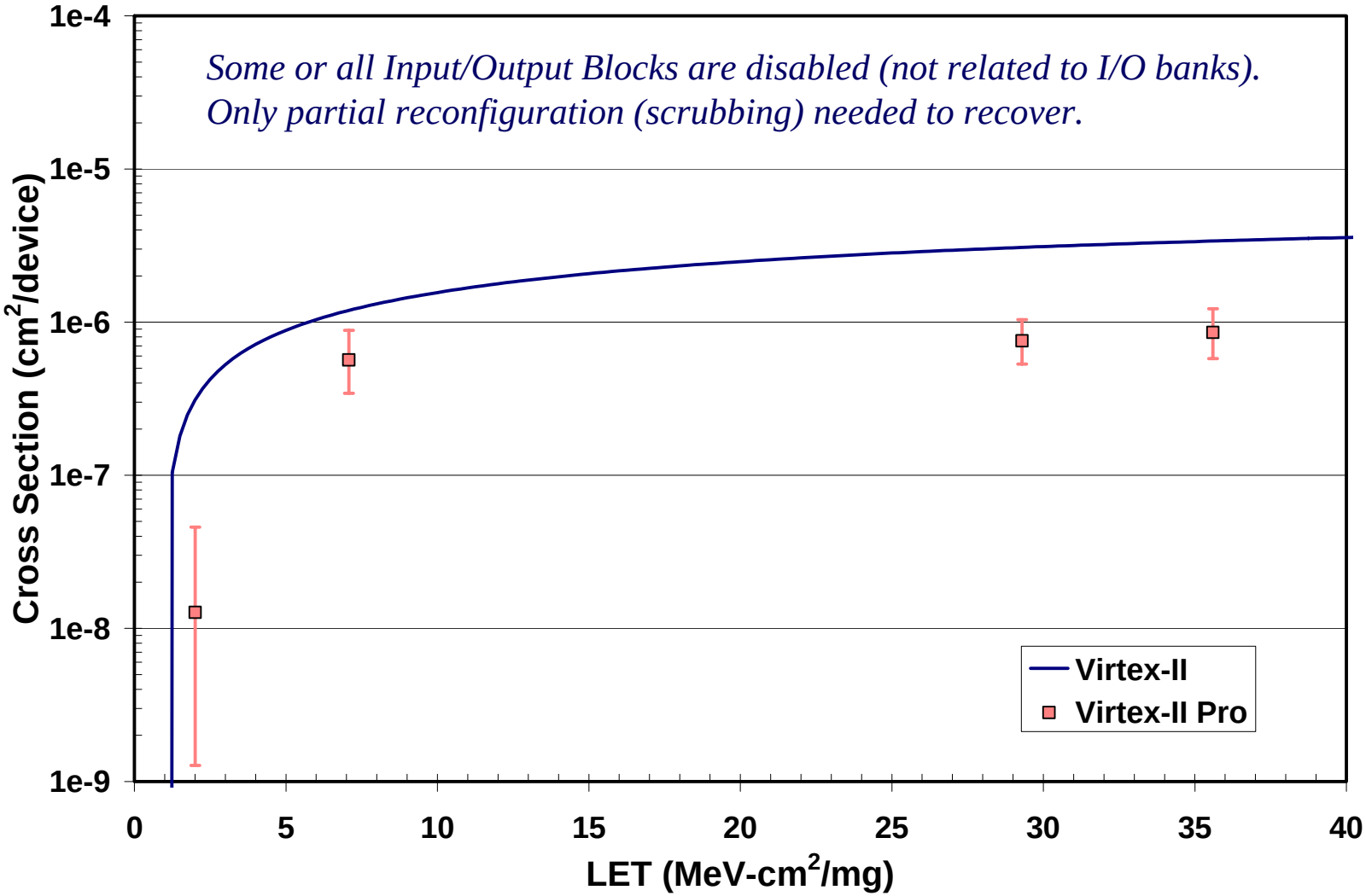
SelectMap SEFI



“Power Cycle” SEFI



I/O “SEFI”


Some or all Input/Output Blocks are disabled (not related to I/O banks).
Only partial reconfiguration (scrubbing) needed to recover.
Cross Section (cm²/device)
1e-4
1e-5
1e-6
1e-7
1e-8
1e-9
0
5
10
15
20
25
30
35
40
LET (MeV-cm²/mg)
Virtex-II
Virtex-II Pro

Summary

- Virtex-II Pro fabric performs better than Virtex-II
  - Configuration logic and BlockRAM both improved
  - Flatter knee region will improve orbital error rates
- Input/Output Block results same as Virtex-II
- SEFI results are very similar
  - IOB “SEFI” markedly improved in Virtex-II Pro
- NEW SEFI mode in Virtex-II Pro
  - Requires power cycle to recover
  - Occurs 5x less often than POR

Additional References

1. “Virtex-II Static Characterization”, Xilinx Single Event Effects Consortium, 2004
2. Gary M. Swift, et al., “Dynamic Testing of the Xilinx Virtex-II Field Programmable Gate Array (FPGA) Input Output Blocks (IOBs),” 2004 Nuclear and Space Radiation Effects Conference (NSREC), Monterey, CA
3. J. Moore, C. Carmichael, G. Swift, J. George, “Single Event Effects (SEE) Test Results on the Virtex-II Digital Clock Manager (DCM)”, 2004 MAPLD.
4. C. Yui, G. Swift and C. Carmichael, “Single Event Upset Susceptibility Testing of the Xilinx Virtex II FPGA,” 2002 MAPLD, Laurel MD, 10-12 Sept. 2002.
5. R. Koga, J. George, G. Swift, et al., “Comparison of Xilinx Virtex-II FPGAs SEE sensitivities to Protons and Heavy Ions,” 2003 RADECS, The Netherlands
6. G. Swift, C. Yui and C. Carmichael, “Mitigating Upsets in SRAM-based FPGAs from the Xilinx Virtex 2 Family,” 2003 MAPLD’03
7. C. Carmichael, “Triple Module Redundancy Design Techniques for Virtex FPGAs, “Xilinx Application Note XAPP197, Nov. 2001.