High Speed Energy Efficient Architectures for Finite Ridgelet Transform

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Over the last decade, Field Programmable Gate Arrays (FPGAs) have gained considerable acceptability as a preferred platform for the implementation of various subsystems onboard satellites, particularly due to reasons of no NRE costs, rapid design cycles and availability of the Rad-Hard FPGAs versions. Moore’s law has allowed FPGAs to graduate from their traditional role of glue logic to high demand applications such as telemetry and onboard data processing. Optical systems and imaging technology deployed onboard satellites has also improved dramatically, with typical data rates of Giga Bits Per Second (GBPS). However, the onboard storage capacity and downlink capacity are constrained by power and total bandwidth available. Inevitably, onboard image compression is the only viable option to overcome these bottlenecks. The choice of lossless vs. lossy compression is motivated by various parameters including volume of image data to be compressed, type of image compressed and acceptable thresholds of perceptual, photometric and astrometric measures.

While wavelets are the popular choice for lossy and near lossless image compression, impressive results can be obtained by employing the FRIT (Finite Ridgelet Transform). FRIT was recently introduced to overcome the limitations of wavelets in higher dimensions. The two fundamental building blocks of Ridgelet are the Finite Radon Transform (FRAT) and the Discrete Wavelet Transform (DWT). The FRAT was first introduced as the finite analogue of integration in the continuous radon transform, with origins in the field of combinatorics. The mathematical representation of an injective (and hence invertible) form of the FRAT applied on finite Euclidian planes is shown below.

\[
 r_k[l] = \frac{1}{\sqrt{p}} \left( \sum_{(i, j) \in L_{k,l}} f[i, j] \right)
\]

where \( L_{k,l} = \{(i, j) : j = (ki + l) \mod p, i \in Z_p\}, \quad 0 \leq k < p, \)

\( L_{p,l} = \{(l, j) : j \in Z_p\} \)

To eliminate rounding errors and for efficient hardware implementation, in the DWT block, an integer version of the CDF(2,2) biorthogonal transform factored via lifting steps has been implemented. Since the FRAT operates on a grid with a side that is prime, symmetric extension is one approach to extend the boundary of the block. In addition to this, a novel approach explored in this paper is to use tiles of FRAT blocks instead, with the side of the tile, \( T \), being large enough for \( N \) levels of decomposition. i.e. \( T = 2^N \times p \).

An important factor that needs to be considered while designing systems for deployment onboard satellites is the Single Event Upsets (SEUs). SEUs can manifest themselves as transient upsets or as static upsets. Provisioning for SEUs is of critical importance for space applications. The conventional design technique of the Triple Modular Redundancy (TMR) or ‘majority vote’ is followed in the proposed design process to mitigate effects of SEU on affecting the Flip flops in the CLBs.

In this paper, a high speed low power Single Event Upset (SEU) tolerant architecture for the FRIT has been presented. The proposed FRIT architecture has been simulated and synthesised on the Virtex-E and QPro Virtex2 Rad Tolerant FPGAs and prototyped on the Celoxica RC1000 PCI development board fitted with the Xilinx Virtex XCV2000E-6 FPGA. The architectures are implemented using Handel-C, a C-like language supporting parallelism, and flexible data size and provide a very powerful method of hardware implementation, which is very useful especially in custom computing applications. Complete implementation details and a detailed analysis of performance metrics including maximum frequency, throughput rate, power and energy consumption will be presented in the full paper.