Design of a ‘Single Event Effect’ Mitigation Technique for Reconfigurable Architectures
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Commercially off the shelf (COTS) available reconfigurable System-on-Chip architectures, are becoming popular for applications where high dependability, performance and low costs are mandatory constraints such as space applications. We present a unique SEE (single Event Effect) mitigation technique based upon Temporal Data Sampling and Weighted Voting for synchronous circuits and configuration bit storage for reconfigurable architectures. The design technique addresses both conventional static SEUs (Single Event Upsets) and SETs (Single Event Transients) based errors which result in data loss for reconfigurable architectures in space. The design technique not only eliminates all the single event upsets and single event transients but eliminates all double event upsets as well.

Keywords: Fault tolerance, SEU, Reconfigurable, System-on-Chip (SoC), Mitigation, SET.

Reconfigurable architectures are becoming increasingly popular with space related design engineers as they are inherently flexible to meet multiple requirements and offer significant performance and cost savings for critical applications. As the microelectronics industry has advanced, Integrated Circuit (IC) design in general and reconfigurable architectures (FPGAs, reconfigurable SoC and etc.) in particular have experienced dramatic increase in density and speed due to decrease in feature sizes with which these devices are manufactured. These advancements have serious implications for the reconfigurable architectures when used in space environment where IC is subject to total ionization dose and single event effects as well. Out of these effects, single event effects are most difficult to avoid in space-borne reconfigurable architectures. Radiation which results into soft errors (SEU and SET) can cause permanent faults, when it hits configuration memory of a reconfigurable System-on-Chip architecture. The configuration bit controls the overall functionality of architecture through routing of a signal as shown in the Figure 1:

![Figure 1: Upsets in Signal Routing](image)

This bit-flip due to SEU or SET remains effective till the time bit-stream (configuration data) is not reloaded (Scrubbing Technique) or not corrected by dedicated hardware. The results from bit-stream fault injection \cite{1} and radiation ground testing \cite{2} have confirmed the efficacy of Triple Modular Redundancy (TMR) structure combines with scrubbing, to recover upsets in the reconfigurable architectures. However, the TMR technique has some limitations, such as area over-head (due to triplication of each component), does not cover SET based faults and voting circuit faults.

Several SEU mitigation techniques have been proposed in the past few years to avoid faults in reconfigurable architectures. SEU hardened circuit may be accomplished through a variety of mitigation techniques, based on redundancy. Redundancy is either provided by Hardware (extra components), by time redundancy (extra execution time) or by a combination of both. Time and Hardware redundancy techniques are largely used in ASIC \cite{3}. Full hardware or time redundancy allows the voting circuits to vote for correct value in presence of single event upsets. The Time redundancy takes the advantage of the transient pulse characteristic to compare the signal’s value at different intervals of time.

In the case of reconfigurable architectures, the problem of finding an efficient technique in terms of area, performance and power is very challenging, because of the high complexity of the architectures. An SEU is classified as a soft fault but has permanent effects in reconfigurable architectures, for example, the SEU can effect routing of a signal by effecting configuration memory and user’s synchronous circuits by effecting the memory elements and combinational circuits. The
consequences of SEU can not be handled through standard ASIC fault tolerant schemes such as Error Correction and Detection Codes (EDAC) or standard TMR with single voter circuits because a fault in encoder/decoder or in voter circuit itself will invalidate the technique. TMR is an attractive scheme for reconfigurable architectures because it provides full hardware redundancy including user’s combinational, sequential circuits, the routing and IO pads. However, TMR has limitations like area overhead, IO pad limitations and power dissipation.

In this work, we propose a novel design technique to cope with both SEU and SET faults. The design technique is based upon temporal data sampling and weighted voting. This design technique not only gives 100% fault recovery from SEU but also gives 100% fault recovery from SET, dual event faults and 50% recovery from triple event faults. The technique reduces the scrubbing frequency to half because it can handle double faults as well and hence, improves the overall performance of the system.

The first key step in our newly proposed technique is Temporal Data Sampling. With the help of this sampling technique, all SETs in the clock and data signals are eliminated.

A simple embodiment of the Temporal Data Sampling is shown in Figure 2. Three different clocks (Clk-A, Clk-B, Clk-C) are used. These three clocks are derivative of the main clock (as shown in Figure 3) and have a phase shift to cope with the SETs based errors.

Majority voting is commonly used in TMR systems. The proposed mitigation technique is based upon unique ‘Weighted Majority Voting’. Each node has been assigned a voting weight based on a rule s “Voting weight of a node is inversely proportional to the probability of that node being disturbed by the radiation”.

The proposed scheme gives immunity against all single faults and double faults as well. Due to this added feature, scrubbing frequency can be reduced which enhances the system performance compared to other techniques. The consideration of using reconfigurable SoC in space is fairly recent and there still a lot of work to be done in this area. The technique proposed can be employed in commercial FPGA’s as well with minimum speed and area overhead.

REFERENCES
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