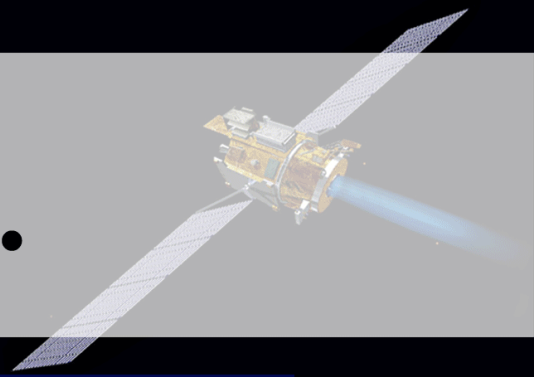
Abstract

We describe a single event functional interrupt (SEFI) mitigation technique that monitors and maintains the operational status of commercial microprocessors in radiation environments. Proton radiation test results using this technique with an Intel Pentium III microprocessor and a Texas Instruments TMS320C6713 DSP processor are presented.

SPACE MICRO INC.



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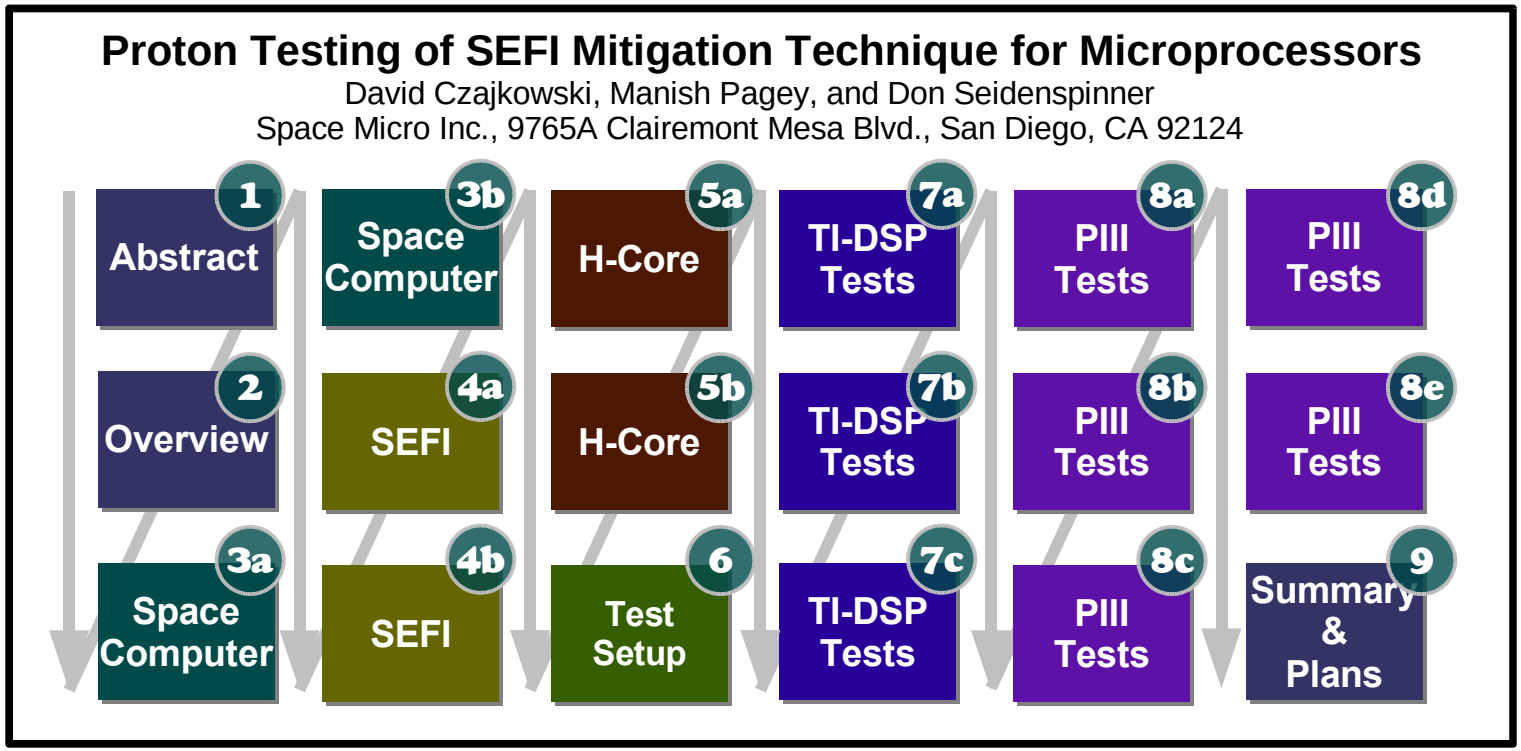
Overview



3a-3b	Proton-100k Space Computer	7a-7c	Tests/Results for TI-DSP Processor
4a-4b	Effects of SEFI on Microprocessors	8a-8e	Tests/Results for PIII Processor
5a-5b	Hardened Core (H-Core) Technique	9	Summary and Future Plans
6	Radiation Experimental Setup		

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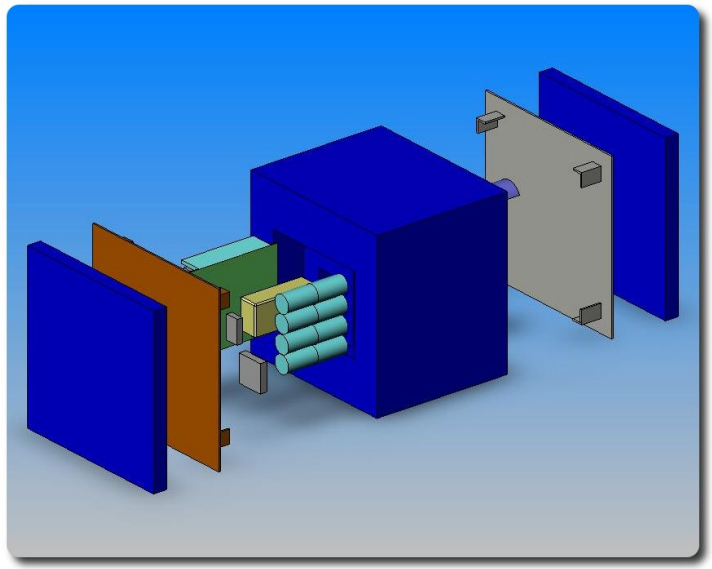
Space Micro Inc. Subsystem Background

SPACE MICRO

- **Rad-Hard satellite computer.**
- **Performance goals:**
  - Over 1000 MIPS throughput,
  - Less than 1 SEU in 1000 days, and
  - Less than 10W power consumption.
- **Building Proton-100k now.**

- **Designed and flew ANTS.**
- **Low space orbit balloon testing.**
- **Successful balloon launch (Dec.'03).**
- **Received real-time data and recovered payload.**



Proton-100k Space Computer

- 2400 MIPS @ 400 MHz
- Over 1440 MIPS with SEU Correction.
- Less than $1x10^{-5}$ uncorrected SEU errors/day.
- SEFI mitigation using H-Core™ Chip.
- No single event latchup.
- Total dose hard to over 100krad(Si).
- 4.9W CPU and 8W total power.
- 1GB/s 64-bit DMA bus.
- PCI/I2C/Parallel bus support.
- 3U cPCI form factor.
- VxWorks and Linux OS supported.

Single Event Functional Interrupts

- **EIA/JEDEC Standard No. 57 (1996):**

  "The loss of functionality of the device that does not require cycling of the device's power to restore operability unlike SEL and does not result in permanent damage as in SEB."

- **SEFIs observed in various complex integrated circuits: EEPROMs, DRAMs, ADC/DACs, Microprocessors.**

- **Most common solution for SEFIs is to power cycle the system:**

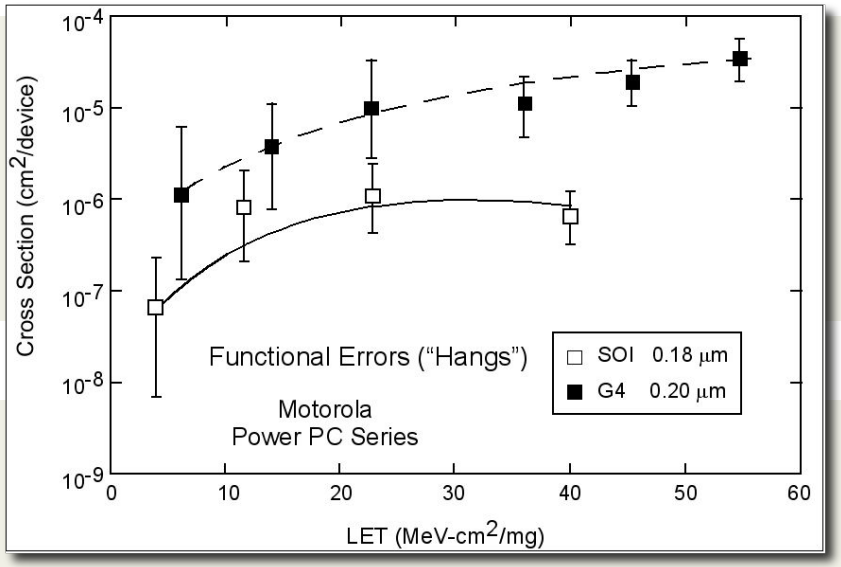
  "Even single bit-flips can create circuit-level effects that cause string of errors, or even result in a "lock-up" condition that requires removal of power and subsequent re-initialization to resume proper operation."

  -K. LaBel et al., "Emerging Radiation Hardness Assurance Issues: A NASA Approach for Space Flight Programs", 1998.

  (http://radhome.gsfc.nasa.gov/radhome/papers/RHA98.pdf)

SEFIs in Microprocessors

- **SEFI Characteristics:**
  - Processor "hangs" suddenly.
  - Observed under proton or heavy ion irradiation.
- **All microprocessors susceptible.**
- **Probable causes of "hangs":**
  - Illegal branching,
  - Upsets in program counter of the CPU, and
  - Jump to undefined/test states.
- **Approx. rates: 1 per 100 days for SOI PowerPC and 1 per 10 days for the CMOS version.**
- **SEFI is a severe problem and not easily solvable.**
- **Current solution to power cycle the system result in unnecessary delays and data loss.**



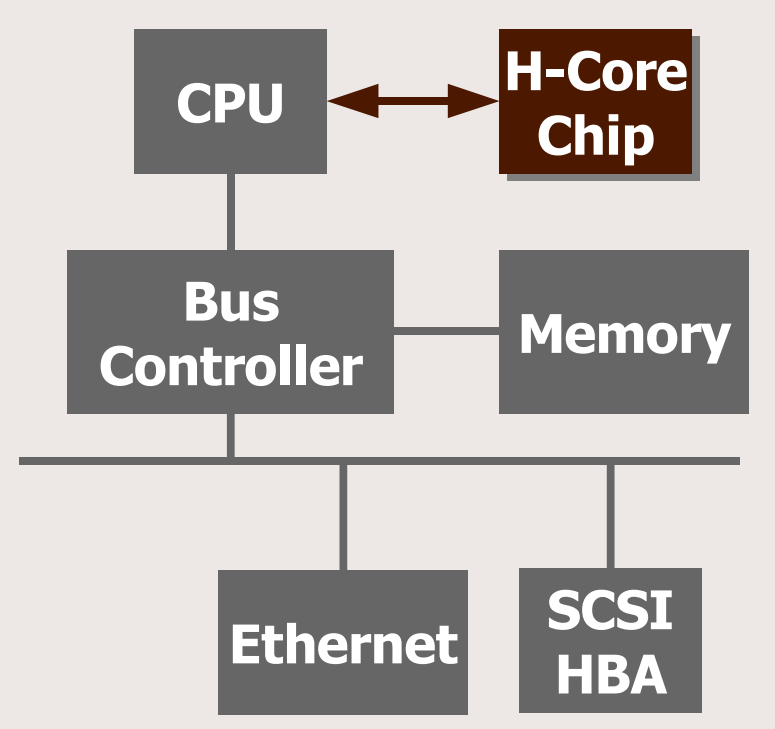
Hardened-Core Technique

Hardened-Core Chip

- Monitors CPU functionality,
- Stores rollback information,
- Detects and indicates SEFI occurrences, and
- Revives CPU from SEFI events.

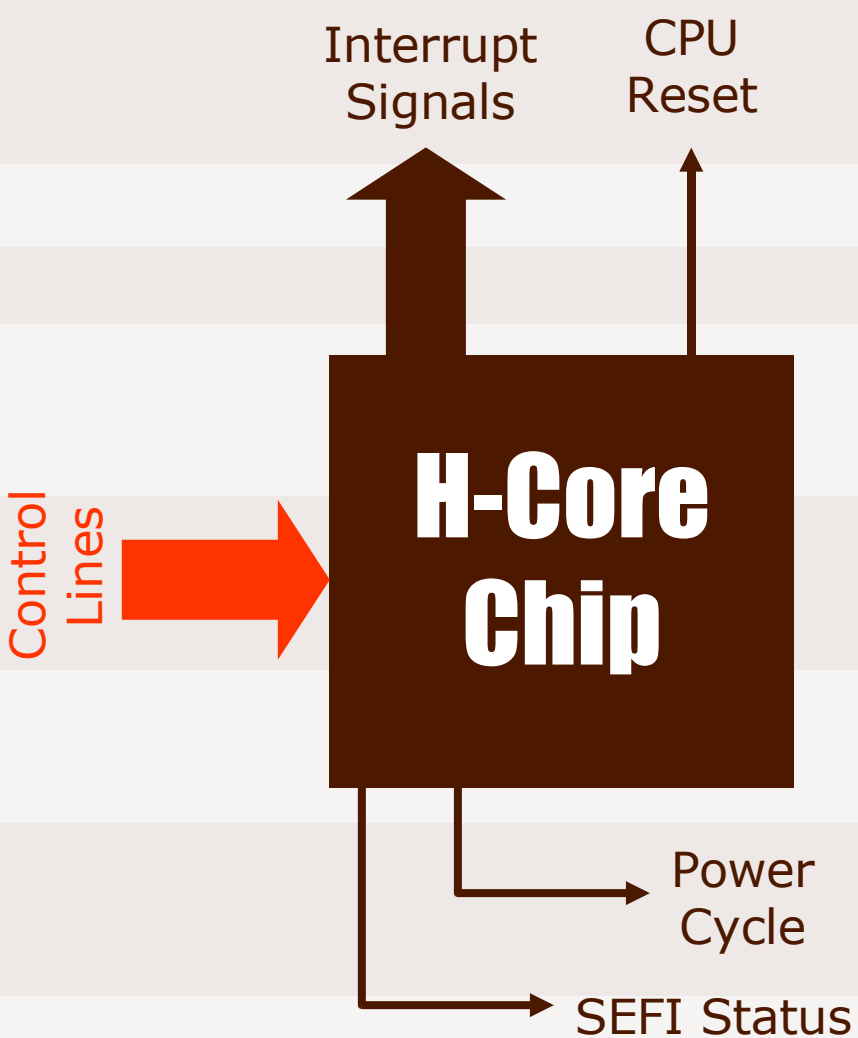
Hardened-Core Software

- Sends "CPU alive" messages,
- Saves periodic roll-back information,
- Reads SEFI indicator from H-Core chip, and
- Recovers running processes after SEFI events.



Hardened-Core (H-Core) is a combination of hardware and software techniques that can detect and recover from SEFIs in microprocessors without power cycle or data loss.

The H-Core Chip



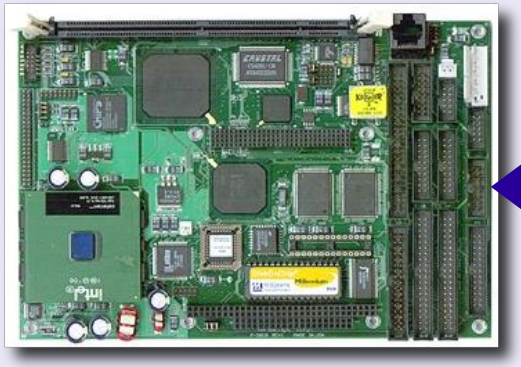
- Manufactured using rad-hard components.
- Usable with any processor.
- Provides min. 8 interrupt signals.
- Uses MOSFET driver for power cycle.
- Provides variable levels and pulse widths of interrupts.
- Contains programmable CPU-check timer.
- Sets SEFI status signal for SEFI recovery software.
- Provides external reset control.

Overview of Radiation Experiments

- **Processors Tested:**
  - 225MHz Texas Instruments TMS320C6713 (TI-DSP)
  - 850MHz Intel Pentium III (PIII)
- **Radiation Facility:**
  - Crocker Nuclear Laboratory at U. C. Davis.
  - Processor irradiated with 51MeV protons.

TI-DSP Experimental Setup

TMS320C6713 DSK



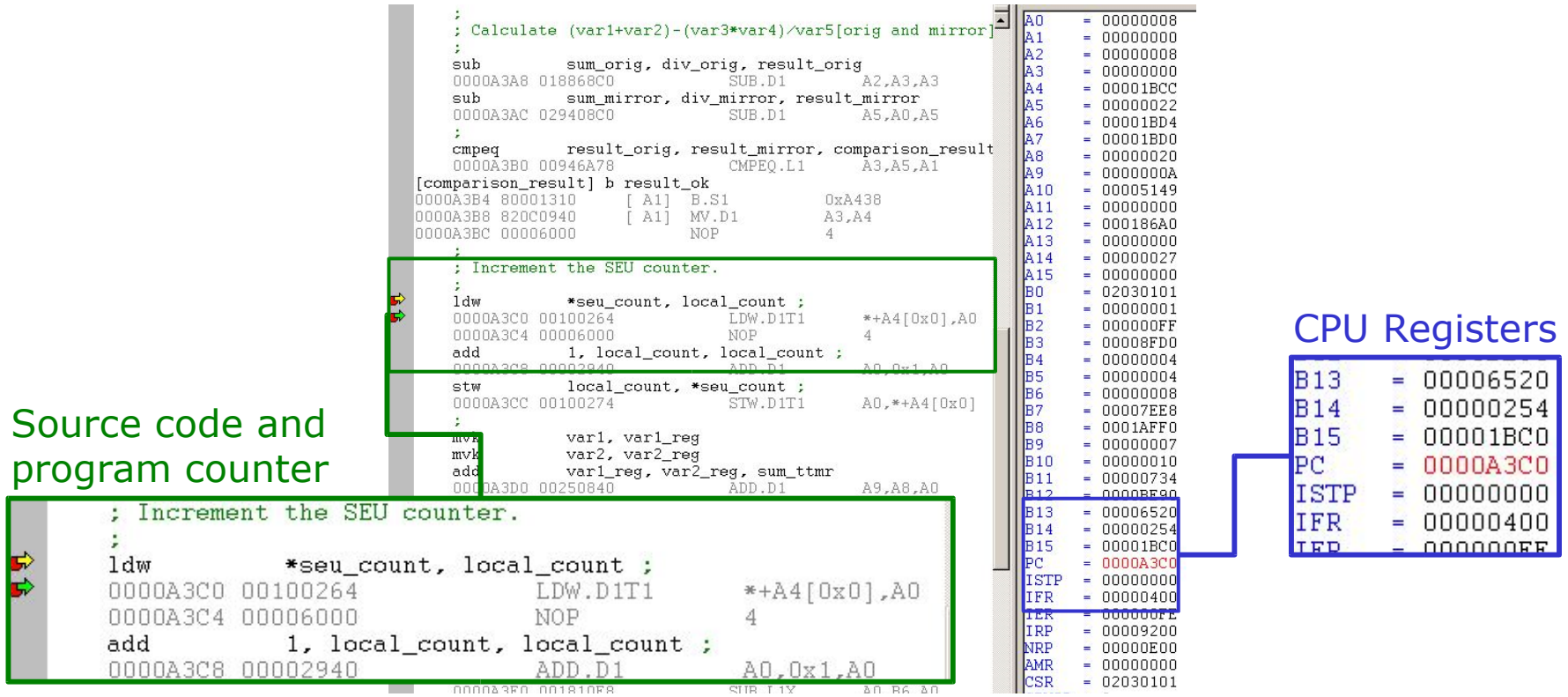
- Development board
- Runs SEFI test loops
- Communicates using USB-JTAG link.

USB

Monitor Computer

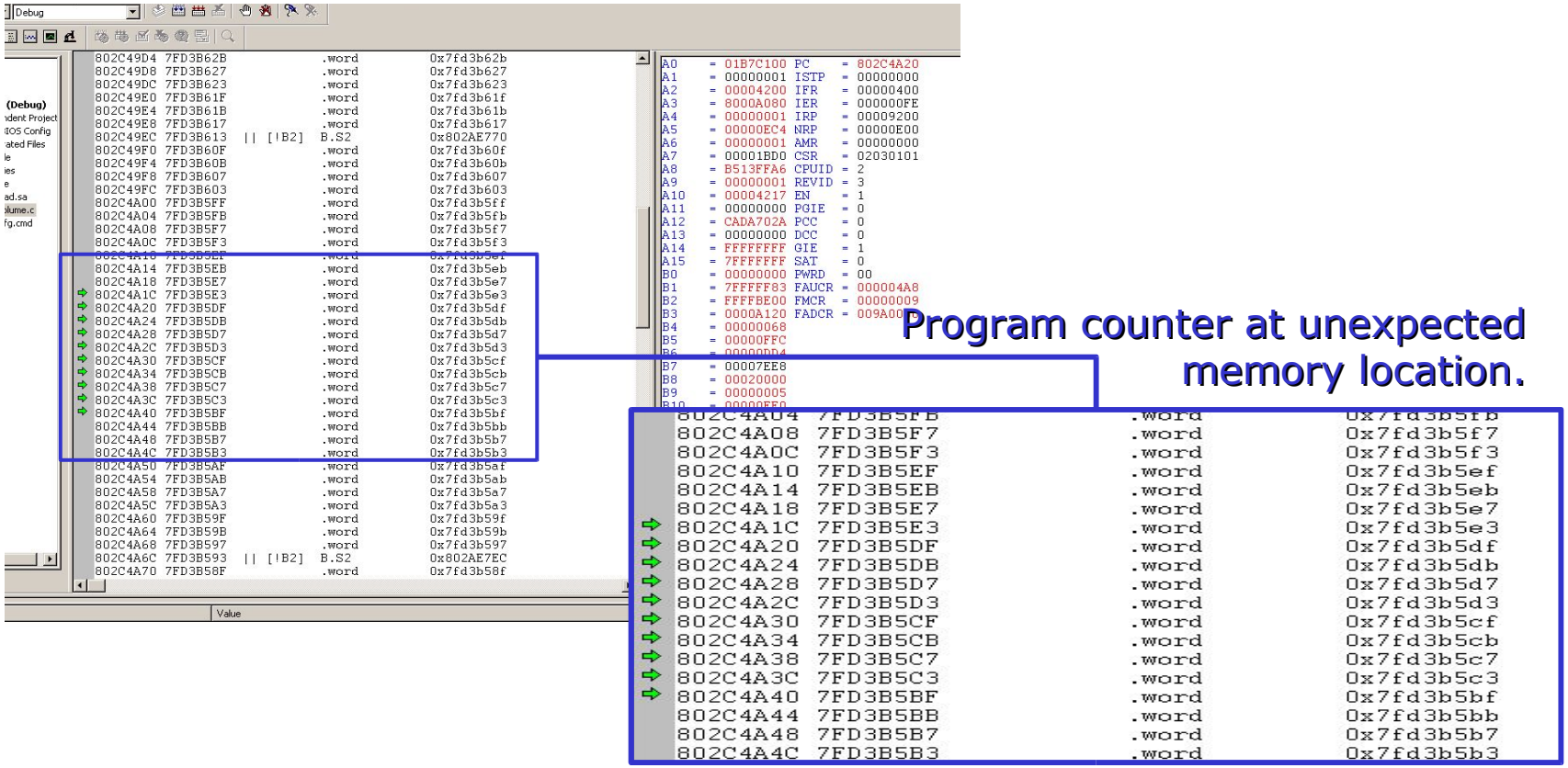
- PC with Windows 2000.
- Uses TI's CodeComposer to communicate with DSK.
- Monitors and controls the TI-DSP board.

Monitoring TI-DSP Execution



- **CodeComposer allows remote monitoring of processor.**
- **All processor registers can be observed during irradiation.**
- **Test loop results are transmitted back to Monitor computer.**

Signatures of SEFIs



- **Typical SEFI signatures observed during radiation experiment:**
  - Jumps to arbitrary memory locations containing random data.
  - Execution of valid instructions that are not part of current program.

Intel PIII Experimental Setup

VSBC-8d Test Computer

- Software/Hardware include:
  - SEFI board and test loop,
  - Diagnostic self-tests,
  - Hardware watchdog, and
  - Linux software watchdog.

RS-232

Serial Console

Ethernet

H-Core Signals

Monitor Computer

- Controls test loops,
- Collects test results, and
- Sends H-Core signals.

Test and Monitor Software

- **VSBC-8d runs Linux OS**
- **Test loops:**
  - Mathematical functions test.
  - CPU timer test.
  - Network communication test.
  - IDE controller test.
- **Monitor software:**
  - Serial console and telnet.
  - Socket communication with test loops.
  - Data logging during irradiation.
  - H-Core signal generation after SEFI.

H-Core Signals for Intel PIII

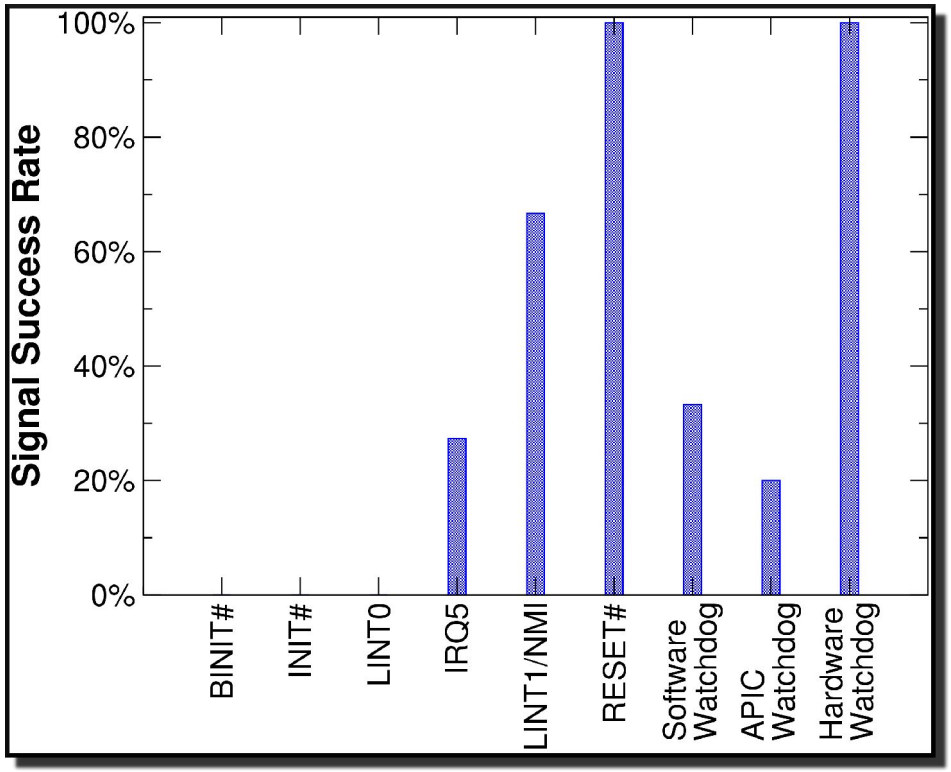
- **BINIT#** — Bus state machine reset.
- **INIT#** — Resets integer registers.
- **LINT0** — General purpose interrupt signal.
- **IRQ5** — Hardware interrupt through PCI bus.
- **LINT1** — Non-maskable interrupt (NMI).
- **RESET#** — Intel PIII hardware reset signal.
- Software, hardware, and APIC watchdogs.

Irradiation Test Procedure

1. Verify test loop results without radiation.
2. Start irradiation and monitor test loop results.
3. Stop irradiation when incorrect/no test loop results received.
4. Assert H-Core signals in sequence to revive the processor.
5. CPU assumed to be fully recovered when it responds to a signal.

H-Core Signal Success Rates

- **SEFI Occurrences and Recovery**
  - 21 SEFIs detected during experiment.
  - 21 SEFIs recovered using H-Core signals.
  - IRQ5, NMI, and RESET# most effective signals.
  - Presence of software/hardware/APIC watchdog aids recovery.



SEFI mitigation using H-Core technique illustrated for Intel Pentium III processor under proton irradiation.

Summary and Future Work

Summary

- Anatomy of SEFI illustrated using proton irradiation of TI-DSP processor.
- H-Core technique developed for SEFI mitigation.
- H-Core signals selected for SEFI recovery of Intel PIII processor.
- Proton irradiation performed on PIII board with H-Core circuit.
- Processor recovered from all detected SEFIs using H-Core signals without requiring power cycle.

Future Work

- Development of recovery software after SEFI detection.
- Proton radiation experiments on multiple processor boards (AMD, PowerPC, and TI-DSP).
- Incorporate H-Core chip in Proton-100k space computer.
- Offer standalone H-Core chip and IP core.