

# Abstract

We describe a single event functional interrupt (SEFI) mitigation technique that monitors and maintains the operational status of commercial microprocessors in radiation environments. Proton radiation test results using this technique with an Intel Pentium III microprocessor and a Texas Instruments TMS320C6713 DSP processor are presented.



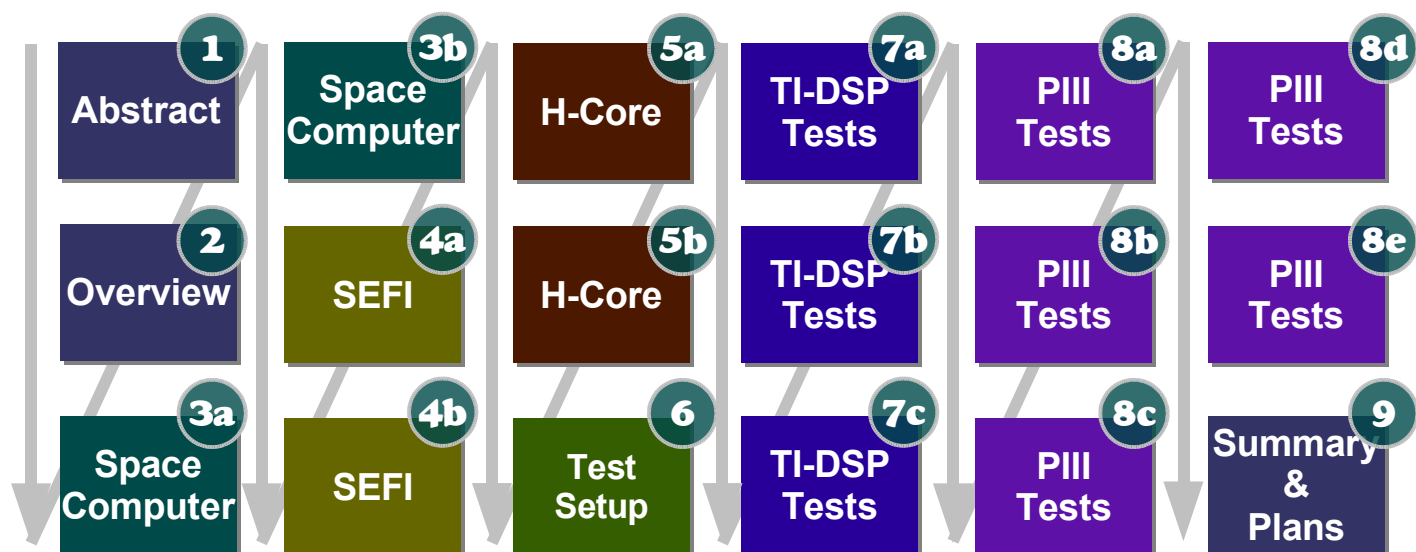
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# Overview

## Proton Testing of SEFI Mitigation Technique for Microprocessors

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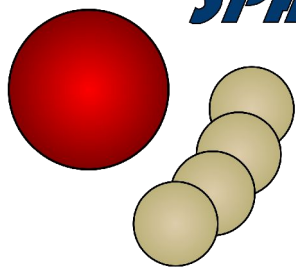
Summary and Future Plans

Project partially funded by NASA MSFC as part of a Phase II SBIR.

# Space Micro Inc.

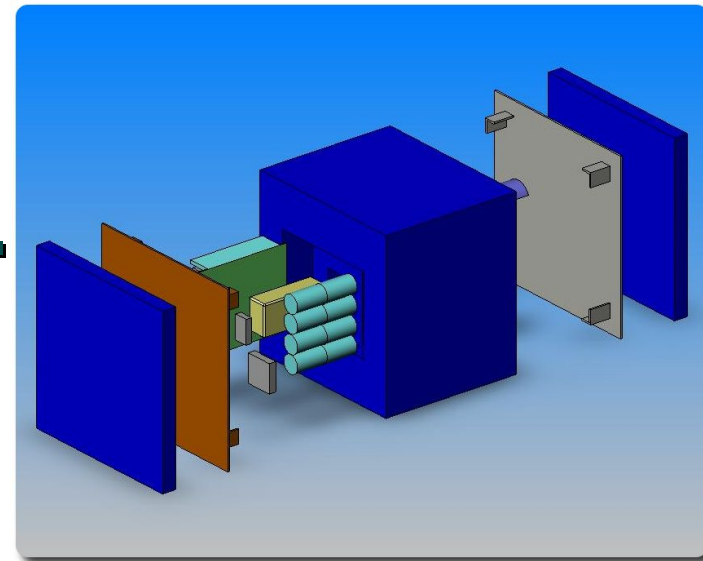
## Subsystem Background

***SPACE MICRO***



- ⊕ **Rad-Hard satellite computer.**
- ⊕ **Performance goals:**
  - ⤴ Over 1000 MIPS throughput,
  - ⤴ Less than 1 SEU in 1000 days, and
  - ⤴ Less than 10W power consumption.
- ⊕ **Building Proton-100k now.**

- ⊕ **Designed and flew ANTS.**
- ⊕ **Low space orbit balloon testing.**
- ⊕ **Successful balloon launch (Dec.'03).**
- ⊕ **Received real-time data and recovered payload.**



# Proton-100k Space Computer

3b

- ⊕ **2400 MIPS @ 400 MHz**
- ⊕ **Over 1440 MIPS with SEU Correction.**
- ⊕ **Less than  $1 \times 10^{-5}$  uncorrected SEU errors/day.**
- ⊕ **SEFI mitigation using H-Core™ Chip.**
- ⊕ **No single event latchup.**
- ⊕ **Total dose hard to over 100krad(Si).**
- ⊕ **4.9W CPU and 8W total power.**
- ⊕ **1GB/s 64-bit DMA bus.**
- ⊕ **PCI/I2C/Parallel bus support.**
- ⊕ **3U cPCI form factor.**
- ⊕ **VxWorks and Linux OS supported.**



# Single Event Functional Interrupts

## ⊕ **EIA/JEDEC Standard No. 57 (1996):**

*“The loss of functionality of the device that does not require cycling of the device’s power to restore operability unlike SEL and does not result in permanent damage as in SEB.”*

## ⊕ **SEFIs observed in various complex integrated circuits: EEPROMs, DRAMs, ADC/DACs, Microprocessors.**

## ⊕ **Most common solution for SEFIs is to power cycle the system:**

*“Even single bit-flips can create circuit-level effects that cause string of errors, or even result in a “lock-up” condition that requires removal of power and subsequent re-initialization to resume proper operation.”*

**-K. LaBel et al., “Emerging Radiation Hardness Assurance Issues: A NASA Approach for Space Flight Programs”, 1998.**

**(<http://radhome.gsfc.nasa.gov/radhome/papers/RHA98.pdf>)**

# SEFIs in Microprocessors

## ⊕ SEFI Characteristics:

- ⬆ Processor “hangs” suddenly.
- ⬆ Observed under proton or heavy ion irradiation.

## ⊕ All microprocessors susceptible.

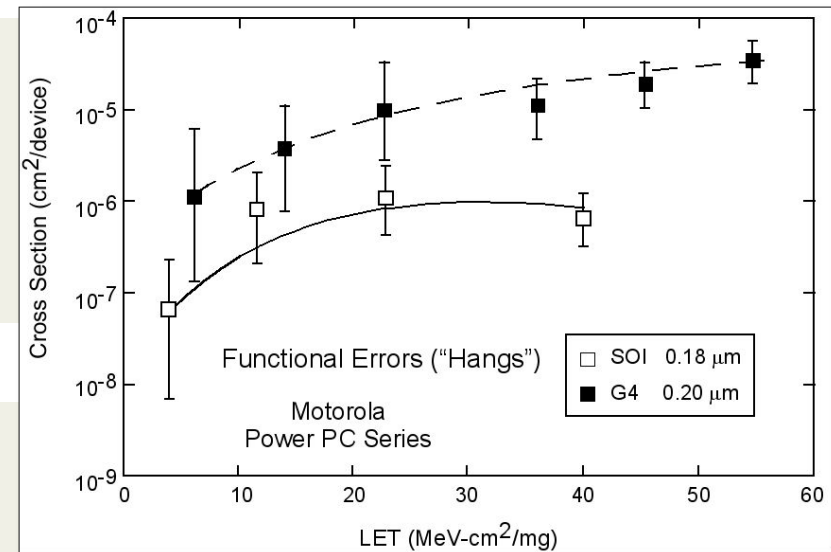
## ⊕ Probable causes of “hangs”:

- ⬆ Illegal branching,
- ⬆ Upsets in program counter of the CPU, and
- ⬆ Jump to undefined/test states.

## ⊕ Approx. rates: 1 per 100 days for SOI PowerPC and 1 per 10 days for the CMOS version.

## ⊕ SEFI is a severe problem and not easily solvable.

## ⊕ Current solution to power cycle the system result in unnecessary delays and data loss.



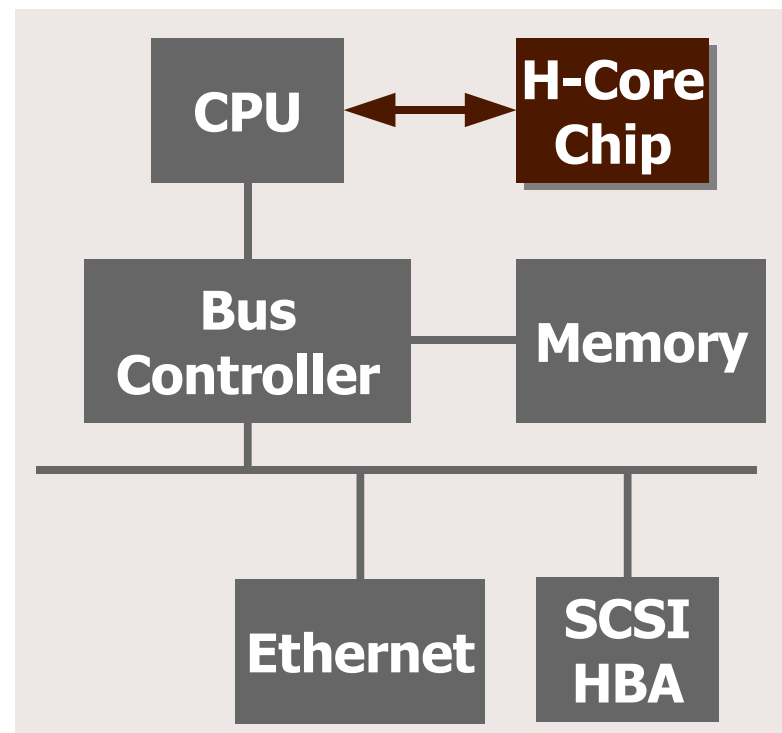
# Hardened-Core Technique

## ⊕ **Hardened-Core Chip**

- ⬆ Monitors CPU functionality,
- ⬆ Stores rollback information,
- ⬆ Detects and indicates SEFI occurrences, and
- ⬆ Revives CPU from SEFI events.

## ⊕ **Hardened-Core Software**

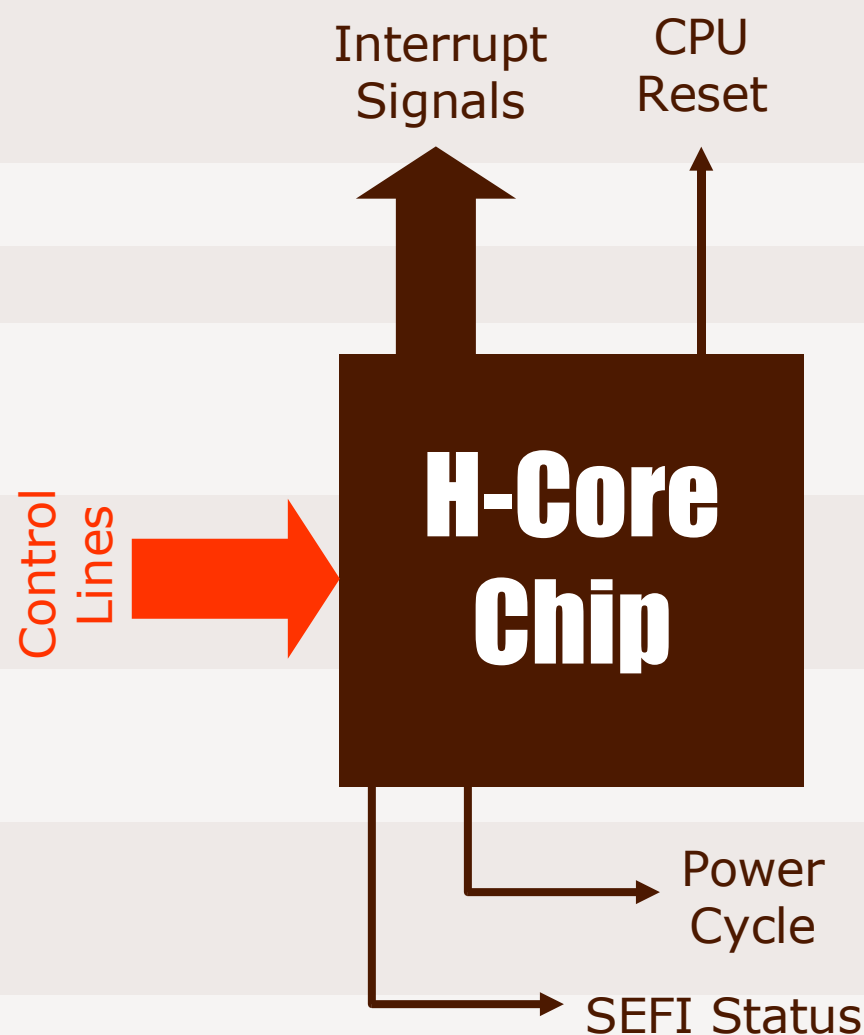
- ⬆ Sends "CPU alive" messages,
- ⬆ Saves periodic roll-back information,
- ⬆ Reads SEFI indicator from H-Core chip, and
- ⬆ Recovers running processes after SEFI events.



**Hardened-Core (H-Core) is a combination of hardware and software techniques that can detect and recover from SEFIs in microprocessors without power cycle or data loss.**



# The H-Core Chip



- ⊕ **Manufactured using rad-hard components.**
- ⊕ **Usable with any processor.**
- ⊕ **Provides min. 8 interrupt signals.**
- ⊕ **Uses MOSFET driver for power cycle.**
- ⊕ **Provides variable levels and pulse widths of interrupts.**
- ⊕ **Contains programmable CPU-check timer.**
- ⊕ **Sets SEFI status signal for SEFI recovery software.**
- ⊕ **Provides external reset control.**



# Overview of Radiation Experiments

## ⊕ **Processors Tested:**

- ⤴ 225MHz Texas Instruments TMS320C6713 (TI-DSP)
- ⤴ 850MHz Intel Pentium III (PIII)

## ⊕ **Radiation Facility:**

- ⤴ Crocker Nuclear Laboratory at U. C. Davis.
- ⤴ Processor irradiated with 51MeV protons.

# TI-DSP Experimental Setup

## TMS320C6713 DSK



- ▲ Development board
- ▲ Runs SEFI test loops
- ▲ Communicates using USB-JTAG link.

USB

## Monitor Computer



- ▲ PC with Windows 2000.
- ▲ Uses TI's CodeComposer to communicate with DSK.
- ▲ Monitors and controls the TI-DSP board.

# Monitoring TI-DSP Execution

Source code and program counter

```

; Calculate (var1+var2)-(var3*var4)/var5[orig and mirror]
;
sub      sum_orig, div_orig, result_orig
0000A3A8 018868C0      SUB.D1      A2,A3,A3
sub      sum_mirror, div_mirror, result_mirror
0000A3AC 029408C0      SUB.D1      A5,A0,A5
;
cmpeq    result_orig, result_mirror, comparison_result
0000A3B0 00946A78      CMPEQ.L1    A3,A5,A1
[comparison_result] b result_ok
0000A3B4 80001310      [ A1] B.S1      0xA438
0000A3B8 820C0940      [ A1] MV.D1      A3,A4
0000A3BC 00006000      NOP      4
;
; Increment the SEU counter.
ldw      *seu_count, local_count ;
0000A3C0 00100264      LDW.D1T1    **A4[0x0],A0
0000A3C4 00006000      NOP      4
add      1, local_count, local_count ;
0000A3C8 00002940      ADD.D1      A0,0x1,A0
stw      local_count, *seu_count ;
0000A3CC 00100274      STW.D1T1    A0,**A4[0x0]
;
movk     var1, var1_reg
movk     var2, var2_reg
add      var1_reg, var2_reg, sum_ttmr
0000A3D0 00250840      ADD.D1      A9,A8,A0
;
; Increment the SEU counter.
;
ldw      *seu_count, local_count ;
0000A3C0 00100264      LDW.D1T1    **A4[0x0],A0
0000A3C4 00006000      NOP      4
add      1, local_count, local_count ;
0000A3C8 00002940      ADD.D1      A0,0x1,A0

```

CPU Registers

A0	=	00000008
A1	=	00000000
A2	=	00000008
A3	=	00000000
A4	=	00001BCC
A5	=	00000022
A6	=	00001BD4
A7	=	00001BD0
A8	=	00000020
A9	=	0000000A
A10	=	00005149
A11	=	00000000
A12	=	000186A0
A13	=	00000000
A14	=	00000027
A15	=	00000000
B0	=	02030101
B1	=	00000001
B2	=	000000FF
B3	=	00008FD0
B4	=	00000004
B5	=	00000004
B6	=	00000008
B7	=	00007EE8
B8	=	0001AFF0
B9	=	00000007
B10	=	00000010
B11	=	00000734
B12	=	0000BEE0
B13	=	00006520
B14	=	00000254
B15	=	00001BC0
PC	=	0000A3C0
ISTP	=	00000000
IFR	=	00000400
IFR	=	000000FE
IRP	=	00009200
NRP	=	00000E00
AMR	=	00000000
CSR	=	02030101

- ⊕ **CodeComposer allows remote monitoring of processor.**
- ⊕ **All processor registers can be observed during irradiation.**
- ⊕ **Test loop results are transmitted back to Monitor computer.**

# Signatures of SEFIs

Program counter at unexpected memory location.

Address	Value	Comment
802C49D4	7FD3B62B	.word 0x7fd3b62b
802C49D8	7FD3B627	.word 0x7fd3b627
802C49DC	7FD3B623	.word 0x7fd3b623
802C49E0	7FD3B61F	.word 0x7fd3b61f
802C49E4	7FD3B61B	.word 0x7fd3b61b
802C49E8	7FD3B617	.word 0x7fd3b617
802C49EC	7FD3B613	[1B2] B.S2 0x802AE770
802C49F0	7FD3B60F	.word 0x7fd3b60f
802C49F4	7FD3B60B	.word 0x7fd3b60b
802C49F8	7FD3B607	.word 0x7fd3b607
802C49FC	7FD3B603	.word 0x7fd3b603
802C4A00	7FD3B5FF	.word 0x7fd3b5ff
802C4A04	7FD3B5FB	.word 0x7fd3b5fb
802C4A08	7FD3B5F7	.word 0x7fd3b5f7
802C4A0C	7FD3B5F3	.word 0x7fd3b5f3
802C4A10	7FD3B5EF	.word 0x7fd3b5ef
802C4A14	7FD3B5EB	.word 0x7fd3b5eb
802C4A18	7FD3B5E7	.word 0x7fd3b5e7
802C4A1C	7FD3B5E3	.word 0x7fd3b5e3
802C4A20	7FD3B5DF	.word 0x7fd3b5df
802C4A24	7FD3B5DB	.word 0x7fd3b5db
802C4A28	7FD3B5D7	.word 0x7fd3b5d7
802C4A2C	7FD3B5D3	.word 0x7fd3b5d3
802C4A30	7FD3B5CF	.word 0x7fd3b5cf
802C4A34	7FD3B5CB	.word 0x7fd3b5cb
802C4A38	7FD3B5C7	.word 0x7fd3b5c7
802C4A3C	7FD3B5C3	.word 0x7fd3b5c3
802C4A40	7FD3B5BF	.word 0x7fd3b5bf
802C4A44	7FD3B5BB	.word 0x7fd3b5bb
802C4A48	7FD3B5B7	.word 0x7fd3b5b7
802C4A4C	7FD3B5B3	.word 0x7fd3b5b3
802C4A50	7FD3B5AF	.word 0x7fd3b5af
802C4A54	7FD3B5AB	.word 0x7fd3b5ab
802C4A58	7FD3B5A7	.word 0x7fd3b5a7
802C4A5C	7FD3B5A3	.word 0x7fd3b5a3
802C4A60	7FD3B59F	.word 0x7fd3b59f
802C4A64	7FD3B59B	.word 0x7fd3b59b
802C4A68	7FD3B597	.word 0x7fd3b597
802C4A6C	7FD3B593	[1B2] B.S2 0x802AE7EC
802C4A70	7FD3B58F	.word 0x7fd3b58f

⊕ **Typical SEFI signatures observed during radiation experiment:**

- ⬆ Jumps to arbitrary memory locations containing random data.
- ⬆ Execution of valid instructions that are not part of current program.

# Intel PIII Experimental Setup

## VSBC-8d Test Computer



- ▲ Software/Hardware include:
- SEFI board and test loop,
  - Diagnostic self-tests,
  - Hardware watchdog, and
  - Linux software watchdog.

RS-232



**Serial Console**

Ethernet



**Monitor Computer**

H-Core Signals

- ▲ Controls test loops,  
▲ Collects test results, and  
▲ Sends H-Core signals.



# Test and Monitor Software

⊕ **VSBC-8d runs Linux OS**

⊕ **Test loops:**

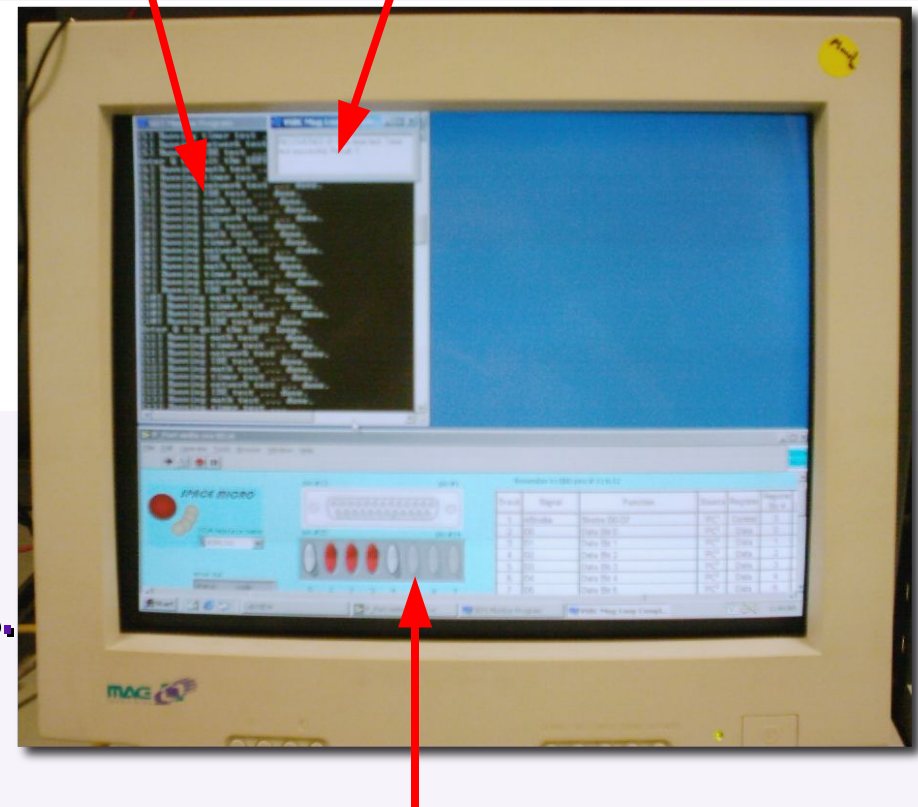
- ⬆ Mathematical functions test.
- ⬆ CPU timer test.
- ⬆ Network communication test.
- ⬆ IDE controller test.

⊕ **Monitor software:**

- ⬆ Serial console and telnet.
- ⬆ Socket communication with test loops.
- ⬆ Data logging during irradiation.
- ⬆ H-Core signal generation after SEFI.

**Monitor software output**

**Test results from VSBC-8d**



**H-Core signal controls**

# H-Core Signals for Intel PIII

⊕ <b>INIT#</b>	<b>Bus state machine reset.</b>
⊕ <b>INIT#</b>	<b>Resets integer registers.</b>
⊕ <b>LINT0</b>	<b>General purpose interrupt signal.</b>
⊕ <b>IRQ5</b>	<b>Hardware interrupt through PCI bus.</b>
⊕ <b>LINT1</b>	<b>Non-maskable interrupt (NMI).</b>
⊕ <b>RESET#</b>	<b>Intel PIII hardware reset signal.</b>
⊕ <b>Software, hardware, and APIC watchdogs.</b>	



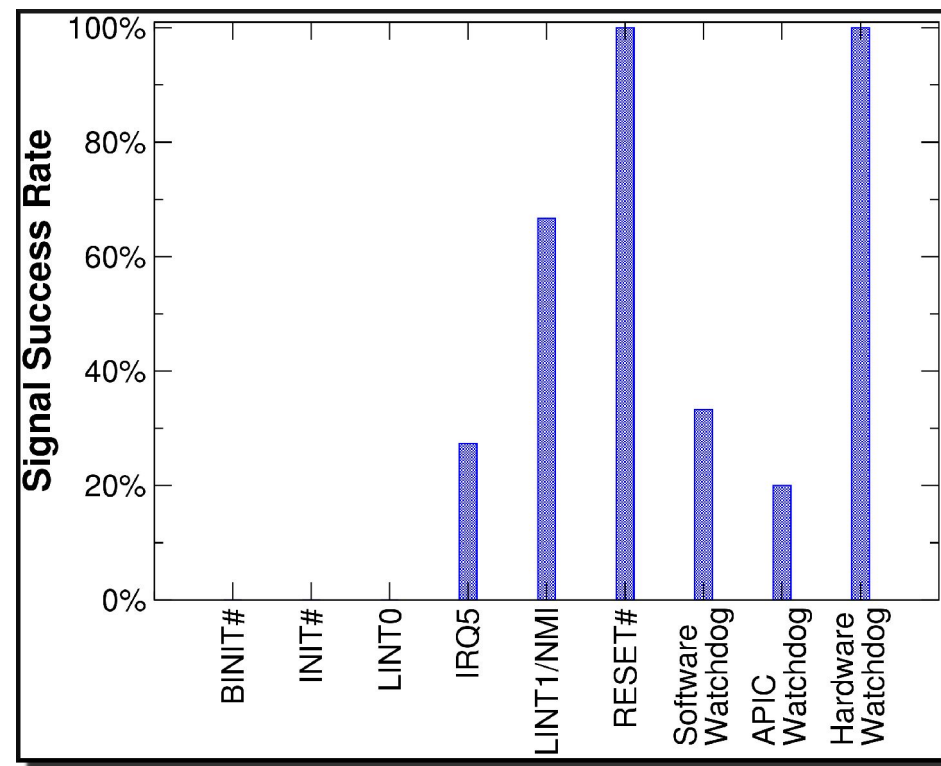
# Irradiation Test Procedure

- 1. Verify test loop results without radiation.**
- 2. Start irradiation and monitor test loop results.**
- 3. Stop irradiation when incorrect/no test loop results received.**
- 4. Assert H-Core signals in sequence to revive the processor.**
- 5. CPU assumed to be fully recovered when it responds to a signal.**

# H-Core Signal Success Rates

## SEFI Occurrences and Recovery

- 21 SEFIs detected during experiment.
- 21 SEFIs recovered using H-Core signals.
- IRQ5, NMI, and RESET# most effective signals.
- Presence of software/hardware/APIC watchdog aids recovery.



**SEFI mitigation using H-Core technique illustrated for Intel Pentium III processor under proton irradiation.**

# Summary and Future Work

## ✦ Summary

- ✦ Anatomy of SEFI illustrated using proton irradiation of TI-DSP processor.
- ✦ H-Core technique developed for SEFI mitigation.
- ✦ H-Core signals selected for SEFI recovery of Intel PIII processor.
- ✦ Proton irradiation performed on PIII board with H-Core circuit.
- ✦ Processor recovered from all detected SEFIs using H-Core signals without requiring power cycle.

## ✦ Future Work

- ✦ Development of recovery software after SEFI detection.
- ✦ Proton radiation experiments on multiple processor boards (AMD, PowerPC, and TI-DSP).
- ✦ Incorporate H-Core chip in Proton-100k space computer.
- ✦ Offer standalone H-Core chip and IP core.