Embedded system for brushless motor control in space application

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Abstract

New space equipments call for higher performance and safety parameters while, at the same time, low system cost. To achieve these specifications this paper presents a Multi Chip Module (MCM) device, named AMBRA (ASIC for BRushless Motor control in space Applications), designed for high performance synchronous brushless motor control in space applications.
The motor control system is realized by arranging an high performances fixed-point DSP core with a set of peripherals optimized for motor brushless based applications.

I. INTRODUCTION

Motion control and positioning of many space mechanisms are accomplished using brushless motors [1]. These motors are used in space applications for their simple and robust construction, high power output to weight ratio, low inertia and optimal performances at high and low speed. Typical applications are scan mirror, thrust vector control actuators, fuel valve control actuators, solar array deployment, control moment gyroscopes, high and low RPM (Rotation Per Minute) applications, light weight applications and low thermal emission applications. Motor control is achieved through a DSP-based fully digital ASIC architecture.
This solution provides, with respect to typical mixed analog-digital control systems, higher flexibility due to the possibility, using a programmable processor, to modify or to update the system; cost reduction and better reliability; drift elimination; greater radiation robustness and less susceptibility to temperature variation and components aging; besides advanced control algorithms can be implemented and control loop delays can be minimized. All these features are highly required in space systems.

The paper is structured as follows: after this brief introduction; Section 2 gives a descriptions of the system components and requirements; algorithms, hardware and firmware overviews are also presented in this section; Section 3 describes the verification and adjustment methodology through a test breadboard while conclusions are drawn in Section 4.

II. SYSTEM DESCRIPTION

AMBRA is a MCM system made up of a digital ASIC, two analog to digital converters and a four double channels multiplexer.
AMBRA system communicates with external devices by an analog interface and some digital ones; in particular encoder, serial, inverter bridge and input/output digital interfaces are present. Figure 1 shows the system block diagram including the motor control external components typically present in a servocontrol system and also used in the test system for the verification of the AMBRA performances: obviously brushless motor, position transducer, position sensor signal conditioning, current signal conditioning and 3-phase inverter providing the required power levels for the brushless motor.

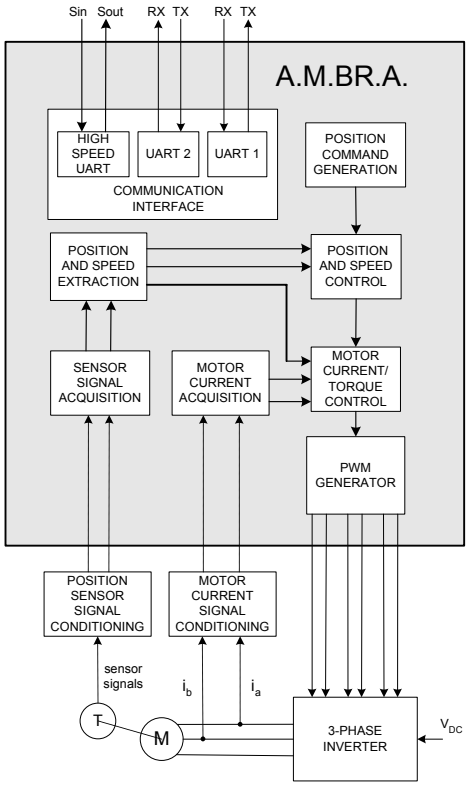

Figure 1 - System block diagram

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The system acquires two of the three motor currents and relative position transducer signals and it provides PWM (Pulse Width Modulation) signals to drive the 3-phase inverter.
The MCM system exchanges data with the external world through the serial communication interface.
Motor current/torque control and position/speed control blocks implement control algorithms, position command generation block provides position commands coming from an external management unit through the serial interface while position and speed extraction block receives data from external transducer and provides position and speed data. Sensor signal acquisition and motor current acquisition have to sample external data with the minimum time skew to reduce errors.

This kind of system calls for the follow system requirements:

- 2-3 kHz current control band
- 21.8 kHz FOC (Field Oriented Control) work frequency
- 3.6 kHz position and speed loop work frequency
- 100 ns analog to digital time conversion
- 12 bit analog to digital resolution.

Implemented algorithms are partitioned between hardware and firmware (DSP) implementations according to the required speed performances, their criticality and flexibility (for instance to cope with possible new system requirements).
For an high updating frequency of control ring the maximum pass band amplitude is required. To this aim current control function are implemented in hardware. High resolution PWM (Pulse Width Modulation) signals generator and serial communication interfaces are implemented in hardware too.
Position/speed extraction and PID (Proportional Integral Derivative) controller are implemented in software because requires less velocity but more flexibility.

A. ALGORITHMS SUMMARY

As showed in figure 1, AMBRA implements a motor position control based on two nested closed loops.
The inner loop is in charge of current and torque controls [2] while the external loop manages the motor position and speed [3].
To achieve aforementioned performances several algorithms have been considered:

(i) PID algorithm to increase dynamic performance in position control; proportional, integral and derivate constants can be fixed by serial interface to ease system set-up.
(ii) trajectory generation to control brushless rotor movement
(iii) position computation to calculate rotor position from resolver data.

The latter being the most critical for the overall system performance. Figure 2 shows implemented architecture for this algorithm using a multispeed x1 x8 resolver.
Input data ENOB (effective number of bit), offset errors and gain mismatch of analog chain highly affect position calculation accuracy. To reduce errors we use an algorithms based on signal oversampling not introducing phase lag, in particular a not uniform 16 points correlation with 3,5 bit ENOB gain.

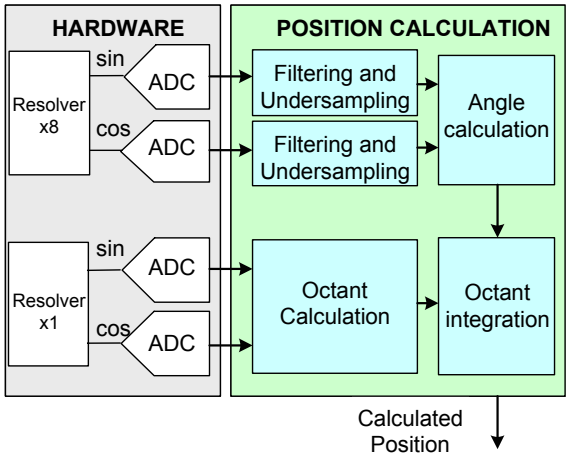

Figure 2 – Position computation algorithm

Algorithms performances, depending on resolver kind, have been evaluated in terms of accuracy, precision and resolution.
With multispeed x1 x8 resolver we have an accuracy of 0.10625 millidegrees, a resolution less then 0.125 millidegrees and a precision of 0.0075 millidegrees.
These algorithms are managed as task in a real-time operative system.
Several algorithms, not concurring to achieve request performances, are implemented in firmware, for example serial communication and tasks management algorithms.

B. HARDWARE OVERVIEW

The fully digital ASIC carries out all the functions for brushless motor control generating 3 PWM channels for driving the MOSFET gates of the inverter bridge to reach the final motor position. The latter is input to the ASIC from the external world through a serial interface.
Two 12 bit - 10 Msps A/D converters are required to simultaneously sample a couple of homogenous signals coming from motor current and sine/cosine signal from the two multispeed resolver winding of the position sensors.
The ASIC architecture, shown in figure 3, was developed as a trade-off between performance, complexity and flexibility. Besides, to ease ASIC testability, which is of paramount importance in space application, a fully synchronous approach was pursued with the exception of the RAMs (Random Access Memories) control logic operating on both clock edges.
ASIC circuit includes a 16 bit - fixed point DSP macro cell. The use of the DSP is required because the control band amplitude is closely connected to real time implementation of the control algorithms and DSP can manage, control and adjust in real time the complex non linear equations building motor dynamic model. This DSP is characterized by 10 MIPS computational power which is more than enough with respect to the figure (estimated in about 7 MIPS) required to perform all the aforementioned

operations, particularly position control and trajectory generation. 70% of DSP resources are involved in cyclic activity, 23% for reference generation, 46% for actual position and speed calculation and 31% for feed forward PID control, the rest are used in acyclic activity.

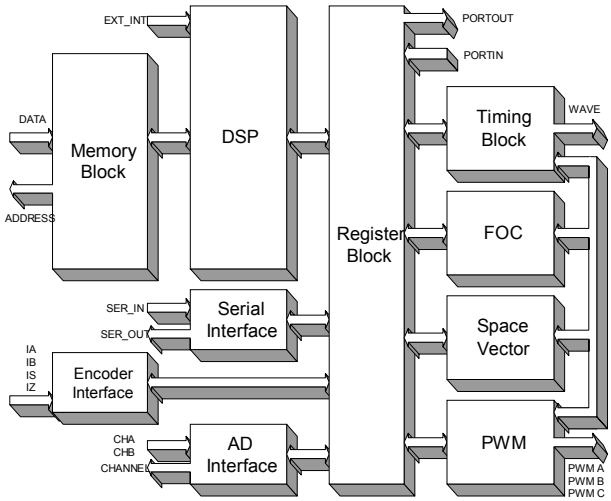

Figure 3 – ASIC architecture

Two RAM data memories 256x16 and a RAM program memory 2048x16 are included.
A FOC [4,5] equipment unit implements direct and inverse Clarke & Park [6] transformation for PID calculation, it comprises the control current ring implementing in hardware current PI control and motor vectorial control algorithm. FOC unit is made up of a sequencer, a 16-bit signed multiplier, an 32-bit signed adder and sequential logic.
The Serial Interface block in Fig. 3, used for debug, performance evaluation and program memory boot, includes an asynchronous UART in addition to the DSP internal synchronous serial interface.
An AD interface is in charge of reading data from AD converter, controlling and compensating data from AD conversion. A Timing Unit produces all timing references necessary for AMBRA system operation, in particular resolver, A/D acquisition, Clarke & Park conversion and PI calculation.
The Register Block interfaces the DSP core with the rest of the circuit; we have three kinds of registers: Setup (writeable by hardware and readable by software), Operational (R/W by hardware at high priority and R/W by software at low priority) and Special. Special registers are seen as simple registers but they perform most complex functions as sine, cosine, arctangent and 32 bit division. Both software and hardware writes them synchronously.
Space Vector block [7] is in charge of controlling the generation of the PWM channels (A, B and C). It's made up of a sequencer, a 16-bit signed multiplier, a 32-bit signed adder, sequential logic and 32 bit divisor.
PWM unit generates the signals for driving the MOSFET gates of the inverter bridge (A, B and C channels). By this unit MOS driving polarity can be inverted.
The Encoder block interfaces an external incremental encoder which is the most used feedback for high performance control systems.
This interface core is a 16 bit quadrature up-down counter which coverts 2 quadrature signals, coming from an external squaring circuit for sine/cosine encoder or directly from a TTL encoder, in a parallel word used by the algorithms.
To improve transportability all the hardware blocks have been described in technology-independent VHDL (Very high-speed integrated circuits Hardware Description Language) code.

C. FIRMWARE OVERVIEW

Rotor position elaboration, position PID control function and FOC reference current generation are implemented in firmware by the selected DSP core. To ease maintenance each functionality has been derived as independent module. We can modify, activate or deactivate modules to change or improve system functionality and performances.
A task manager oversees all module operations in a preemptive mode; figure 4 shows the firmware modules scheduling.
We have three kind of module:

(i) One shot : executed once or in special situations;
(ii) Low priority : performing not critical functions;
(iii) High priority which performs functions of vital importance for system activity.

For each group the modules are executed in circular priority. The modules are divided into two different cycles, in PWM cycle FOC calculates signals for PWM and MOS commands are generated while Resolver cycle is the resolver excitation waveform period and it contains an integer number of PWM cycles.

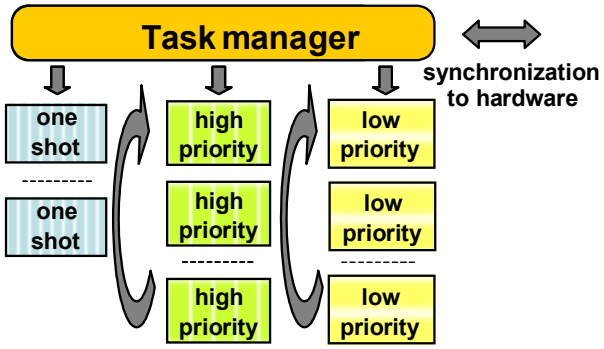

Figure 4 – Firmware modules scheduling

The developed tasks are:

(i) Filter, for resolver signal filtering, improves signal to noise ratio to increase significant bits number;
(ii) Position calculation, the most critical task because directly influences position accuracy;
(iii) PID controller guides system response to external stimulus;
(iv) Trajectory calculation is an optional task to drive motor trajectory during movement;
(v) Serial communication manages protocol between controller and host system.

Every PWM cycles contains two of the aforementioned tasks, the modules are synchronized as shown in Figure 5.

Resolver cycle	PWM cycle	Filter
		Position calculation 1
	PWM cycle	Filter
		Position calculation 2
	PWM cycle	Filter
		PID controller 1
	PWM cycle	Filter
		PID controller 2
	PWM cycle	Filter
		Serial communication
	PWM cycle	Filter
		Trajectory calculation

Figure 5 – Firmware modules synchronization

III. VERIFICATION METHODOLOGY

Before ASIC foundry run, the overall design has been verified and adjusted through rapid prototyping on a customarily designed breadboard; figure 6 shows the breadboard block diagram. The latter features a Xilinx XC2V4000 FPGA, a RS232 interface, two A/D converters, a permanent magnet 3-phase motor with resolver, a 3 phase MOS bridge with relative driver and analog interface modules. The AMBRA circuitry required 33% of the overall FPGA resources (13% due to the DSP core). Several tests have been implemented; system test of PI control current evaluating step response gives a rise time of 90 µs and a current band 2.8 kHz which satisfied the request performances.

Proper test vectors have been developed to verify the functionality of the prototyped system.

In particular the following main tests have been successfully executed:

(i) test program loading into DSP program memory;
(ii) DSP initialization of ASIC registers;
(iii) particular position and current values simulation;
(iv) DSP position computation;
(v) full FOC cycle execution;
(vi) DSP reading of FOC cycle results;
(vii) computed values verification.

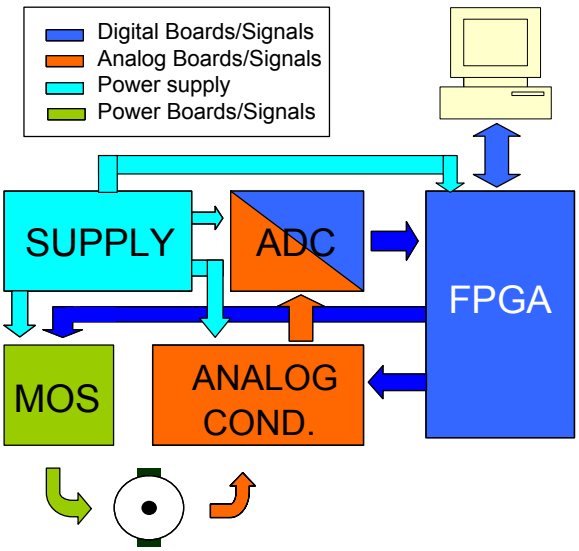

Figure 6 – Breadboard block diagram

The same will be applied to the final system featuring the AMBRA ASIC when back from the silicon foundry.

IV. CONCLUSIONS

After the successful verification of the breadboard prototype, the ASIC design was finalized by means of logic synthesis for the 0.35 µm CMOS Austriamicrosystems technology.

The rationale behind this choice is to allow technology access through reduced-price multi-project wafer and at the same time reduce risks in case of technology retargeting to a radiation tolerant technology such as the 0.35 µm CMOS provided by ATMEL (MH1RT) for the final flight hardware.

The final chip, whose layout is shown in Fig. 7, has 144 PADs; 67 inputs, 47 outputs and 30 power supply PAD (15 Vcc – 15 Gnd). The chip resulted to be PAD limited with an overall area of 19.901 mm^2, a clock frequency of 20 MHz and an estimated power consumption of 226.3 mW @ 3.3 V power supply.

Fault coverage is greater than 97%. MCM is built on 1.6 mm FR4 substrate with tracks and isolations of 100 µm. MCM dimensions are 37x37 mm (connectors included). It's build up of two 12-Bit A/D converters assembled on the substrate in SSOP-28 packages, with 10 MSPS power computation and conversion time less then 50 ns and an analog multiplexer 4:1 - 2 channels in narrow SO-16 package. The aforementioned devices can be replaced by space-qualified ones in the final flight hardware.

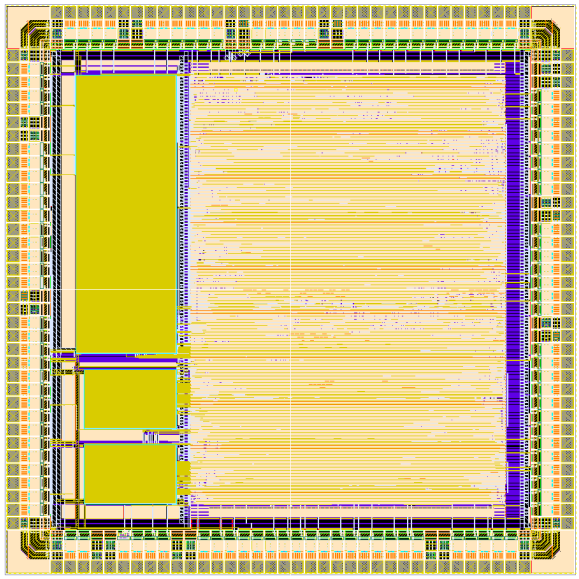

Figure 7 – ASIC layout

System accuracy performances depend on the kind of used resolver. In the prototyping breadboard where we adopted a multi-speed (x1 x8) resolver, the AMBRA position precision amounts to 19 bit.

Summarizing, the main features of the presented AMBRA motor control system are:

(i) great reduction in the number of devices and consequent size and cost reduction;

(ii) increase in the overall reliability due to the fully digital approach;
(iii) radiation, temperature and aging robustness;
(iv) efficient control make it possible to reduce torque, ripples and harmonics and to improve dynamic performances in all speed range;
(v) higher system flexibility and reduced design time/efforts due to a DSP-core based system.

Particularly, the latter allows system re-use in many other applications based on actual position sensors (sine/cosine encoder).

V. ACKNOWLEDGMENTS

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