DC/DC Switching Power Converter with Radiation Hardened Digital Control Based on SRAM FPGAs

F. Baronti, P.C. Adell, W.T. Holman, R.D. Schrimpf, L.W. Massengill, A.F. Witulski, M. Ceschia

Abstract*— The design of a DC/DC switching boost converter based on a radiation hardened digital controller implemented in SRAM FPGAs is presented. Single event functional interrupts (SEFIs) are the dominant radiation effects in SRAM-based FPGAs. When applying digital control using SRAM FPGAs in a switching converter application, SEFIs result in missing pulses in the generated PWM control signal of the converter that cause large transient drops at the converter output. Therefore, we have developed and applied a radiation-hardness-by-design technique based on a logic duplication approach at both the logic and device levels and on a non-disruptive resynchronization mechanism, which ensures the continuous operation of the converter in the presence of radiation induced SEFIs. The proposed RHBD technique is validated with both VHDL simulations and experimental results.

***Index Terms*—DC/DC power converter, boost converter, digital control, single event functional interrupt (SEFI), radiation-hardness-by-design (RHBD).**

I. INTRODUCTION

DC/DC switching power converters, due to their high-efficiency conversion, are essential parts of the power conditioning system of a satellite [1], [2]. The aim of this work is to present the design of a radiation hardened FPGA-based digital control system for a boost converter. Digital control systems have significant advantages over conventional analog pulse width modulators (PWMs) [3], [4]. Indeed, along with the general advantages of a digital system (such as high flexibility, reduced sensitivity to noise and component parameter variations, and the capability to realize sophisticated control algorithms), a digital controller can be hardened more easily against radiation-induced errors than its analog counterpart. In fact, a conventional PWM switching converter is very susceptible to single-event effects (SEEs) in the error amplifier stage and in the analog PWM controller that cause large transient pulses at its output [5]-[7].

The use of commercial SRAM-based FPGAs in space applications is very attractive because of their high component density, quick turn-around time, and reconfigurability [7], [9]. However, SRAM-based FPGAs are very sensitive to SEEs. The dominant effect is the single event functional interrupt (SEFI) caused by a configuration memory bit upset that disrupts the continuous operation of the system in which the FPGA is used. Heavy ion testing on these devices has shown that no permanent faults occur after an SEFI, and that reprogramming the FPGA will restore full functionality [10], [11]. Therefore, "radiation hardening by design" (RHBD) techniques based on detecting, mitigating and correcting SEFIs make it possible to use SRAM-based FPGAs in space applications [12].

The paper is organized as follows. Section II describes the design of a digitally controlled switching boost converter. In Section III the main radiation effects on SRAM FPGAs are discussed. In section IV, the technique applied to harden the design against radiation-induced errors is illustrated. Section V shows the simulated and experimental results, and section VI concludes and summarizes the work.

II. DIGITALLY CONTROLLED BOOST CONVERTER

A DC/DC switching boost converter steps up an unregulated input voltage to a regulated output voltage for a wide range of input voltages and load conditions. The circuit uses an inductor, a power MOSFET, and a diode to transfer power from the input to the output in an efficient way. The MOSFET transistor is periodically switched from the on state to the off state and vice versa. The ratio between the on-state time interval and the switching period (duty cycle) determines the DC value of the output voltage. To maintain the required output voltage in the presence of variations in the input voltage and load conditions, a feedback network, which controls the duty cycle, is used [1].

Figure 1 shows the basic structure of a digitally controlled DC/DC switching boost converter in which the feedback loop is implemented using an analog-to-digital converter (ADC)

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and an SRAM-based FPGA. The actual output voltage $v(t)$ is divided by the sensor gain (H) and converted into a digital signal $v_q[n]$ by means of a sampling process and analog-to-digital conversion (ADC). The difference between the digitized sample of the converter output and the reference voltage (N_{ref}) forms an error signal $e[n]$ that is processed by the digital regulator to calculate the actual duty cycle $d[n]$. Eventually, the digital pulse width modulator (DPWM) generates the switching signal $d(t)$ that controls the power MOSFET.

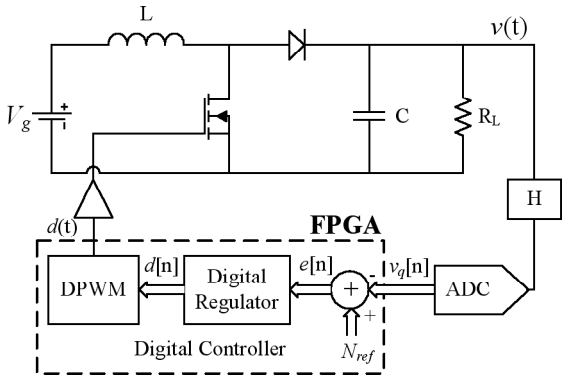

Fig. 1. Basic schematic of a digitally controlled boost converter.

In our design, we applied a 1-bit error resolution technique that uses a deadzone comparator to perform the A/D conversion and a simple up/down counter to calculate the actual duty cycle as shown in Figure 2. This approach avoids the use of an ADC, giving the advantages of a simple design and low power consumption. The use of a deadzone comparator prevents undesired oscillations at the converter output that are unavoidable using a simple comparator [4]. The basic idea, which underlies the advantages of the feedback loop with the deadzone comparator, is that when the error signal enters the deadzone both the up and down inputs of the counter are deactivated and thus the value of the duty cycle is frozen. In this way, when the output voltage approaches the desired value, the loop gain is reduced and a stable operating condition is obtained [14].

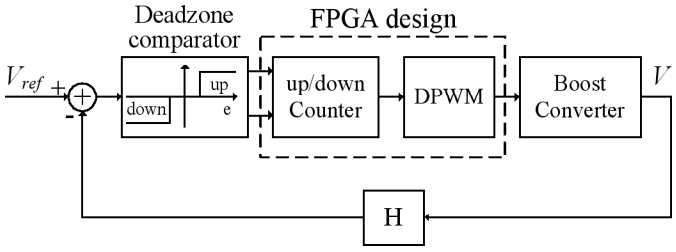

Fig. 2. Block diagram of the designed boost converter.

III. Radiation effects on SRAM FPGAs

Heavy ion testing on SRAM FPGAs from different semiconductor manufactures has shown that these parts are very sensitive to radiation-induced errors [9]-[11]. The dominant error is the single event functional interrupt, which is caused by a configuration memory bit flip. For instance, in the case of the Altera EPF10K100, the measured LET threshold for SEFI is very low (0.1-0.5 MeV-cm^2/mg) [10]. It is worth noting that a user flip-flop is as susceptible as a configuration memory cell to radiation-induced upset. However, the number of configuration bits is much greater than that of the user flip-flops and thus the probability of an SEFI is significantly greater than the probability of an SEU (single event upset) associated with a user register.

Moreover, no permanent faults, such as single event latch-up or dielectric rupture, have been observed during heavy ion tests. In addition, reprogramming the FPGA will restore the full functionality of the device, after the occurrence of an SEFI. Therefore, RHBD techniques based on detecting, mitigating and correcting SEFIs make it possible to use SRAM FPGAs in space applications [12], [13].

IV. Radiation hardening

When applying a digital control signal using an SRAM-based FPGA in a switching converter, radiation induced SEFIs result in missing pulses in the generated PWM control signal of the converter. In turn, the missing pulses result in large transient voltage drops at the output of the converter that may adversely affect the operation of the powered systems [5], [6]. Therefore, an RHBD technique must be applied to mitigate and correct the SEFIs. In the work described here, a redundant approach at both the logic design and the device levels has been applied.

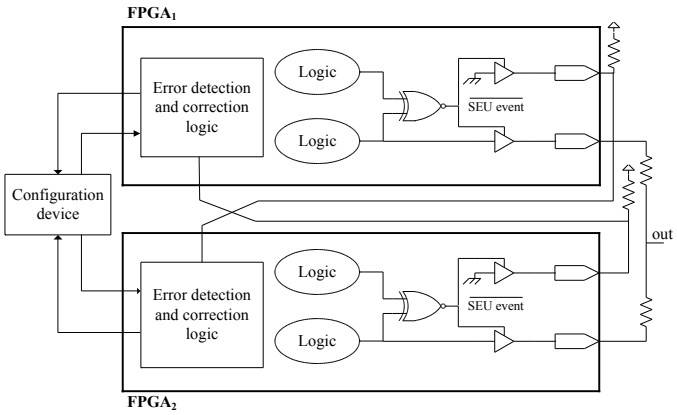

Fig. 3. Basic block diagram of the proposed RHBD technique. Two FPGAs, each of them containing two copies of the same design, are used to mitigate and correct SEFIs. The configuration device allows restoration of the correct configuration bitstream after the occurrence of an SEFI.

As shown in Figure 3, the outputs of two identical logic blocks inside each FPGA are continuously compared to each other using an XNOR gate. An error in either logic block due to an SEU in a user register or an SEFI in the related configuration bits will deactivate the tri-state output buffers of the FPGA. Consequently, the failed device goes in an offline status in which all its outputs are in a high impedance state. A temporary data upset due to an SEU in a user register will

quickly disappear, and the two logic blocks will resynchronize. However, a configuration bit SEFI will result in continuous disagreement between the two logic blocks. The remaining FPGA continues to generate the correct outputs, so that the continuous operation of the overall system is guaranteed.

The recovery from an error condition due to an SEFI is achieved by a cross-checking procedure. Each FPGA continuously monitors the operating state of the other FPGA. If an incorrect operating condition is detected, the failed device is reconfigured. The SEFI detection can be performed by reading back the actual configuration data and comparing it with the original configuration bit-stream. However, this approach relies on a particular feature available only on Virtex FPGAs. A more general approach was applied based on the detection of the offline status of an FPGA through the use of a watchdog counter. The expiring counting value can be set so that an error due to a temporary upset, such as a user register flip, does not force the reconfiguration of the FPGA.

Unfortunately, a reconfiguration alone is not sufficient to restore the system to full functionality because the two FPGAs must resynchronize their current operating states. The simplest way to achieve this is by means of a general reset. However, a reset will disrupt the current state of the system, and an undesirable transient pulse will result at the DC/DC converter output. To avoid this transient error, the logic block was designed so that the reconfigured device can load the current state of the system from the device that is still operating.

V. VHDL SIMULATIONS AND EXPERIMENTAL RESULTS

In order to validate this approach a proof-of-concept demonstration was implemented using Altera FPGAs from the FLEX10K family. An error injection block, as shown in Figure 4, is used to simulate the occurrence of an error in a logic block, and a reconfiguration emulator block is used to emulate the reconfiguration phase. The reconfiguration emulator module forces the output of the related device to a high impedance state during the configuration period, and at its end forces a reset of the device.

Figure 6.a shows the VHDL simulation of the overall system. Note that after the injection of an error in $FPGA_1$, $FPGA_2$ detects the incorrect status of the first device through the offline signal and forces its reconfiguration. During the reconfiguration and the resynchronization phases, the second device generates the correct PWM waveform, and at the end of those phases the reconfigured device restarts operation with the correct duty cycle. The detection of an SEFI occurrence in $FPGA_1$, and its consequent incorrect status, is achieved by $FPGA_2$ through the expiration of its internal watchdog timer, which is no longer reset when the offline signal of $FPGA_1$ becomes active. This mechanism is shown in Figure 6.b.

Figure 5 shows the measured converter output waveforms after the injection of an error (which occurs at $t = 0$) for a conventional design and for the RHBD design. Note that an SEFI causes an unacceptable transient in the converter output, which can be eliminated by applying the proposed RHBD technique. The experimental results confirm that a general reset cannot be applied to resynchronize the two FPGAs after the occurrence of an SEFI because it produces an unacceptable drop of the converter output.

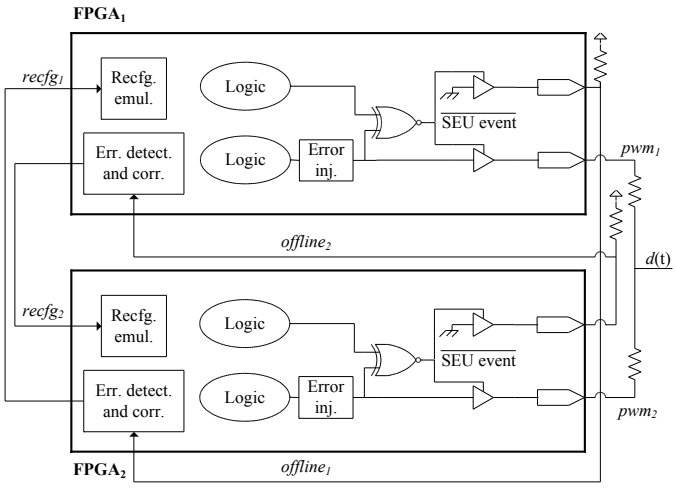

Fig. 4. Representation of the test-bed architecture of the digital controller. The configuration device has been replaced by the internal reconfiguration emulation (Recfg. emul.) block. The error injection module simulates the occurrence of an SEFI.

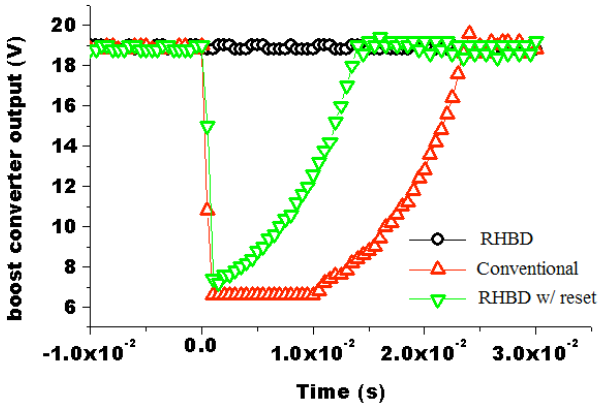

Fig. 5. Measured converter output transients after the injection of an error in both conventional and RHBD designs.

VI. CONCLUSION

Single event functional interrupts are the dominant radiation effects in SRAM-based FPGAs. This work demonstrates the design of an SEFI-hardened DC/DC switching power converter (boost topology) based on a reconfigurable digital control loop implemented in SRAM FPGAs. A dual-redundant self-mitigating technique has been applied to mitigate and correct SEFIs. Moreover, an efficient non-disruptive procedure has been applied to resynchronize

the two FPGAs after the occurrence of an SEFI. The design has successfully been validated through both VHDL simulations and experiments.

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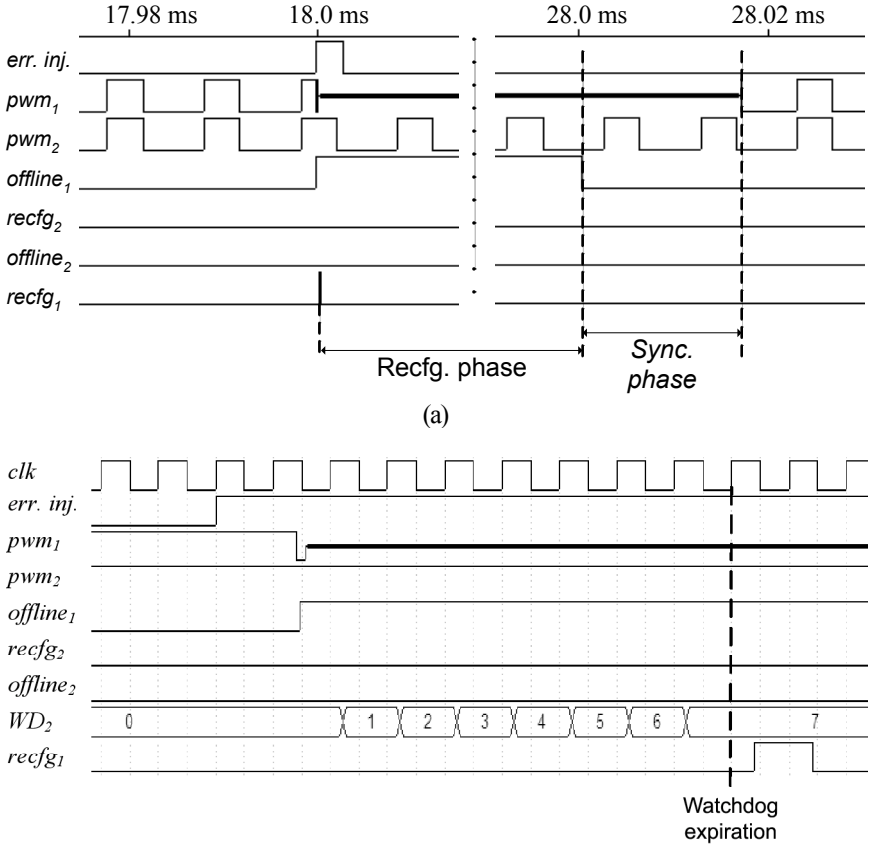

Fig. 6. (a) VHDL simulation of the overall system (b) Detail of the VHDL simulation, showing the expiration of the 3-bit watchdog timer of the FPGA2 after the occurrence of a SEFI on the $FPGA_1$.