Reliability Improving Approach with Opto-Based Voting System

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Abstract

Although SRAM type FPGA has many advantages for space application, it still has a problem that its configuration or stored data may be lost by SEU. To mitigate such negative effects, we have proposed triple voting system with soft core processors [1]. This system provides us both flexibility and reliability in space computers by using SRAM type FPGA in combination with anti-fuse type one.

In this system, three processor cores are implemented on a single SRAM type FPGA and all of their outputs are connected to the voter on an auti-fuse type FPGA. A shared memory is located outside the voter, so all the memory accesses are voted. A voter also accounts for detecting SEU error and identifying the module where SEU occured. This system provides us some advantages such as flexibility and reliability, while it has some disadvantages which may limit the system performance. First, in order to detect and correct SEU errors, all the signals from each modules should be voted in bitwise manner, so this architecture needs large number of wire connections and voter modules. Second, as all the signals among each modules must be synchronized at the voter, we should pay attention to wiring delay of every signals. As a consequence, the operating frequency of the system and system performance has been limited by these points.

Today, similar problem arises from commercial-off-the-shelf (COTS) computer industry. The faster bus operating speed becomes, the more difficult to decrease clock or signal skew to synchronize the signals in the parallel bus. These backgrounds promote almost all the buses in COTS computers going to be serial. All the interfaces between the devices such as memory or other peripherals are likely to be serialized in the near future. This is because serial connection frees us from skew management or signal synchronization, and this approach actually has achieved satisfactory results.

In this paper, we decided to employ serial memory bus in our triple voting system to make it easier to manage signal synchronization. The serial bus contributes in simplifying system configuration and saving resources of the system. Only a few voter modules and simple wire connections are necessary. Moreover, this kind of simplification helps us to avoid many bugs or troubles that result from complicated wire connections. In addition, some FPGAs begin to provide embedded high speed serial interface. For example, VirtexII pro that produced by Xilinx provides such serial interface called Rocket I/O. So we decided to implement the serial memory bus into our triple voting system, planning that we will utilize these devices in the future.

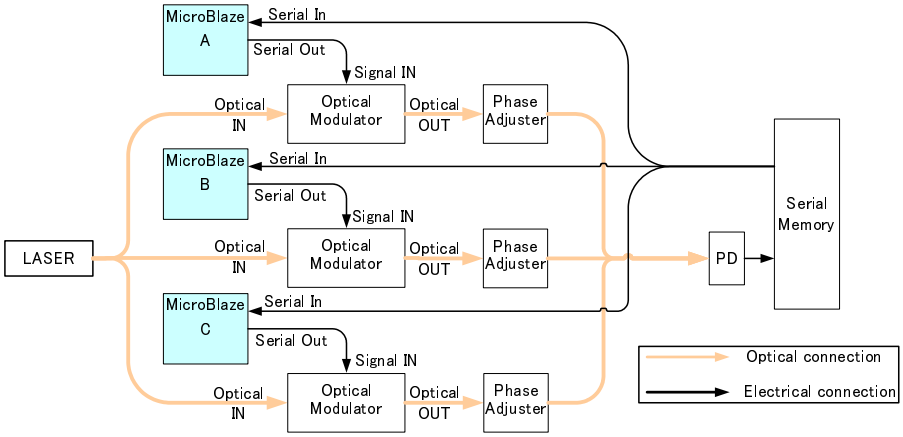

Figure 1: Optical Voting System

In this paper, we discuss the issues that we should consider when we want to implement the serial memory bus with these embedded serial transceiver and propose optical voting system which will be suitable for the high speed serial bus.

The overall architecture assumed in this paper is shown in Figure 1.

This optical voting system consists of three CPU modules which include SER/DES(Serializer/Deserializer) modules in them, three optical modulator, three phase adjuster, a laser diode, a photo detector and a serial memory. Each CPU module is connected to optical modulator. This module modulates AM to the light signal from the LD by electric "0"/"1" signal at very high speed (over *10GHz*). In this system, parallel memory bus is serialized by the SER/DES module in each CPUs firstly. Then, these three serial signals are converted into optical signals at the modulator. After that, the phase of each optical signal is aligned through the phase adjuster and mixed together. Here, three modulated signals interfere each other. Finally, the mixed light wave is converted into electrical signal again by photo detector. This detector changes its output voltage in proportion to the irradiation of input optical signal. If we set proper voltage as a threshold to determine logical high/low output at the photo detector, it can decide the logical output by majority among three serial outputs. Figure 2 shows the concept of this voting technique.

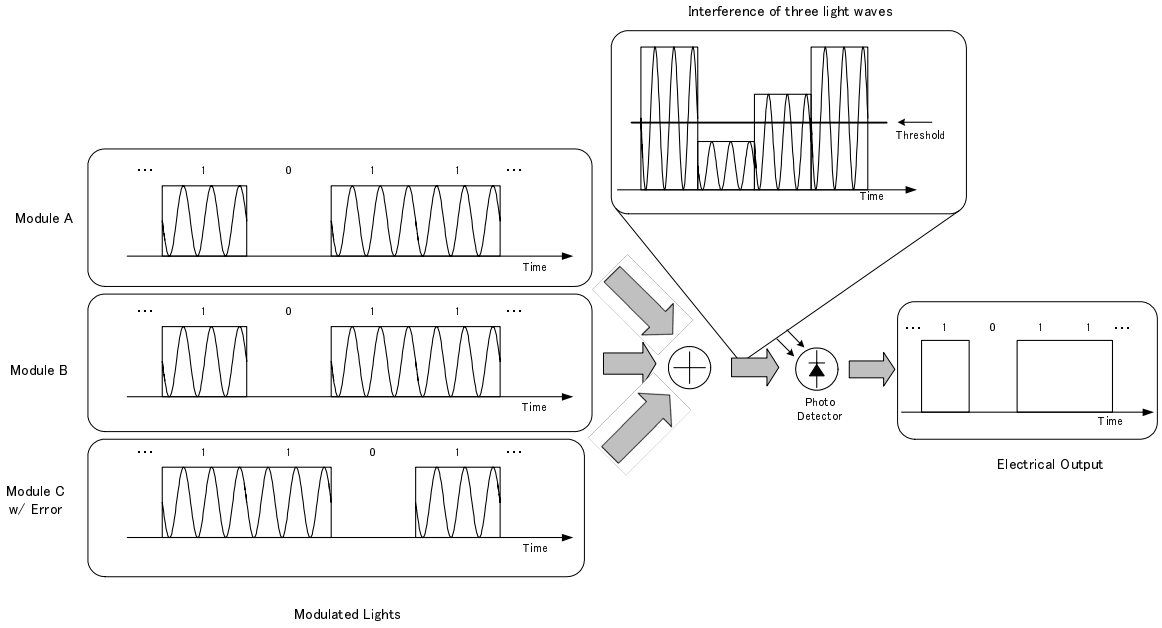

Figure 2: Majority Vote by Amplitude Modulated Optical Signals

We also show the result of evaluating this optical voting system.

References

[1] T.Takahara, Y.Kurahashi, T.Mizuno, H.Saito, and N.Tomita. Embedded Computer System with Soft Core CPU for Space Application. In *Proc. of the 6th International Conference on Military and Aerospace Programmable Logic Device*, 2003.