# Soft errors in adder circuits

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Soft errors in combinational circuits are catching up with errors in memory elements [1]. Continuous device scaling and increasing pipeline lengths contribute to the increase in soft error rates in data-path structures. Thus a detailed evaluation of soft errors in various components of data path is essential.

In logic circuits, an error is caused when the pulse generated by the particle is latched on at the output. In this case, the critical charge ($Q_{critical}$) can be defined as the minimum charge required to latch on to the pulse. There are three masking effects in combinational circuits that affect the propagation of any given pulse to be latched on by the latch or flip-flop at the end of the pipeline stage in a data path. *Logical masking* determined by structure directly depends on the input patterns while *electrical masking* is the function of the inherent delays of logic gates in the circuit. *Latching window masking*, which is a function of the flip-flop set-up and hold time, also determines the timing vulnerability of a node in the circuit apart from determining the $Q_{critical}$. The timing vulnerability ($t_v$) of a node is defined as the fraction of the clock cycle in which a current pulse at the $Q_{critical}$ gets latched on to the output.

This work analyzes soft error rates in adder circuits, which are important components of data path. A detailed analysis of the various masking effects in combinational circuits is done in the case of two prefix adders, Brent-Kung (BK) and Kogge-Stone (KS) adders and they are compared with a Ripple Carry (RC) adder. These are common adder designs used in present day processors. All circuits in our experiments are custom designed and laid out in 1V, 70 nm CMOS Berkeley Predictive technology [2] and simulated using HSPICE [3]. The nodes that are chosen for soft error injection are those that affect the carry chain and are outputs or inputs of the basic cells for better abstraction. An exponential current pulse is injected and is similar to the one modeled in [4].

From the experimental results (Figure 1), it is seen that the $t_v$ (not shown here) along with $Q_{critical}$, determines the occurrences of multi-bit errors in adder circuits. The $t_v$ of the node in turn is affected by the paths to various outputs. Thus from the results, the BK adder has more nodes that will cause multi-bit errors as these nodes have balanced paths to the various outputs and hence has comparable $Q_{critical}$ for all the outputs. The KS adder has lesser number of nodes that have balanced paths to the outputs. For example in Figure 1, pulse at node C1 does not affect S3 and hence does not have a $Q_{critical}$ value. Also, due to shorter carry chains, $Q_{critical}$ values for KS adders are lesser than that for BK.

Voltage and frequency scaling have been widely used to optimize both memory elements and logic circuits for power savings. Understanding the effect of such scaling on soft error rates is important for choosing proper error correction techniques. Here, the designs are simulated with 1V, 0.8V, and 0.6V supplies and frequencies of 1, 0.75 and 0.5GHz respectively. As seen from Figure 2, as voltage scales, the $Q_{critical}$ values reduce and hence result in higher soft error rate.

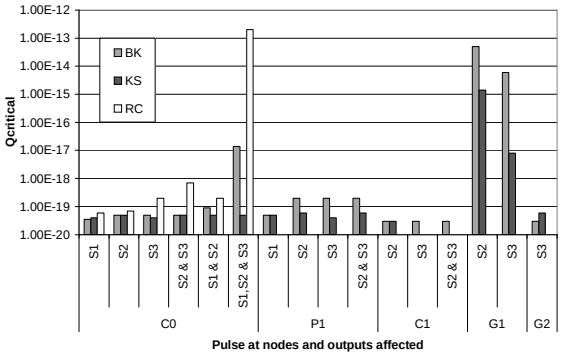


**Figure 1 Comparing Qcritical for BK, KS and RC adders**

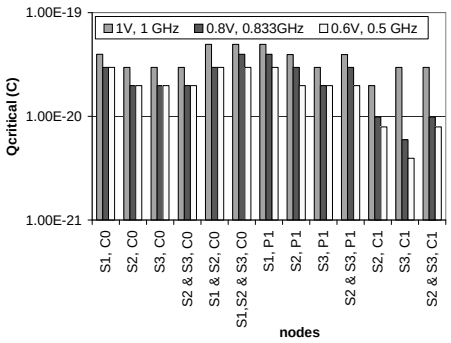


**Figure 2 Effect of scaling voltage and frequency on $Q_{critical}$**

Next, only the frequency is scaled up having a constant voltage and it is found that the $Q_{critical}$ decreased (not shown here) for a few nodes. This is because at higher frequencies, the ripple effect caused due to the carry chain adds on to the required $Q_{critical}$, thus reducing the overall $Q_{critical}$ value. Consequently, scaling down frequency will increase the $Q_{critical}$ and $t_v$, thus resulting in both power savings and reduction in soft error rate while scaling down both voltage and frequency proves to be detrimental for soft error rate though it results in large power savings.

Soft error rate can be reduced by improving either the $Q_{critical}$ (by increasing it) or the timing vulnerability (by decreasing it) of the nodes in adder circuits. We show that $Q_{critical}$ of the nodes in the adder circuits can be increased by increasing the threshold voltage of the logic components along with that of the flip-flops. But we also find that the $t_v$ of the nodes increase as threshold voltage increases and hence trade-off needs to be attained to choose a suitable change in the threshold voltage.

To decrease the timing vulnerability, we show that using a Semi-Dynamic Flip-Flop (SDFF) is better than a Transmission Gate Flip-Flop (TGFF). Since the SDFF has a lesser set-up time than a TGFF, the timing vulnerability of the nodes decreases. This also lowers the number of multiple bit errors occurring in the circuit due to single particle hits.

More detailed results and analysis will be presented in the final version.

## Reference:

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