FFT Mapping on MathStar's FPOA™ FilterBuilder ™ Platform

Pius Ng and David Zhao
MathStar, Incorporated

Abstract*—*MathStar's FilterBuilder Platforms are massively parallel processor arrays built with MathStar's Field Programmable Object Array (FPOA) technology. With a 1 GHz operating frequency and a re-programmable high-bandwidth internal fabric, it is ideally suited for high-performance signal processing such as Software Defined Radio (SDR) and Synthetic Aperture Radar (SAR).

Index Terms*—*Field Programmable Object Array (FPOA), Fast Fourier Transform (FFT), Reconfigurable Architecture.

I. Technology Overview

A MathStar FPOA platform (Figure 1) is a heterogeneous array of Silicon Objects (SOs) interconnecting by a homogeneous reconfigurable network. (Figure 2) The existing SO core library consists of ALU-TruthTable, Register File, State Machine, CAM, and Multiply-Accumulate. Internal block RAM, external SDRAM controller, LVDS with dynamic deskew, GPIO, and configurable SerDes are available in the peripheral library.

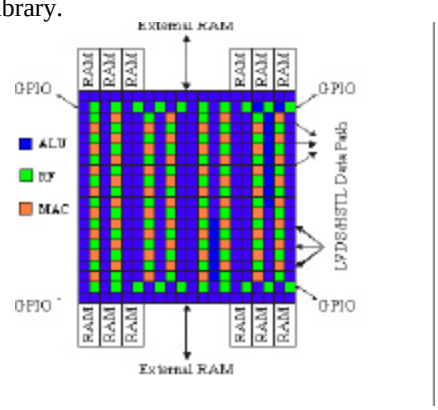

Figure 1: MathStar FPOA FilterBuilder Platform

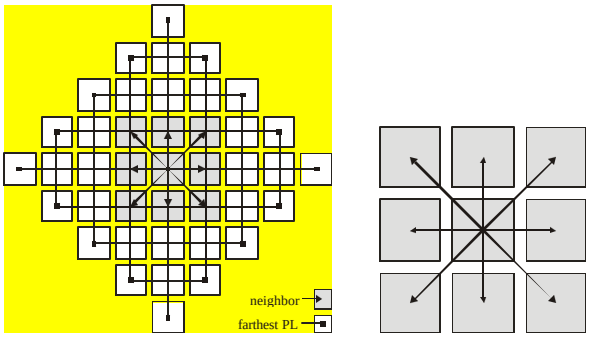

Figure 2: Reconfigurable Interconnect Network

II. Program Development Model

At present, the programming model remains manual in nature. This process is shown in Figure 3. The Summit Visual Elite (VE) Environment provides a graphical IDE for design entry and simulation. The MathStar COAST assists the assignment of objects in use into the valid locations of the platform chosen. The MathStar Object Compiler assembles the design from VE along with assignments generated by MathStar COAST into the binary stream for device programming.

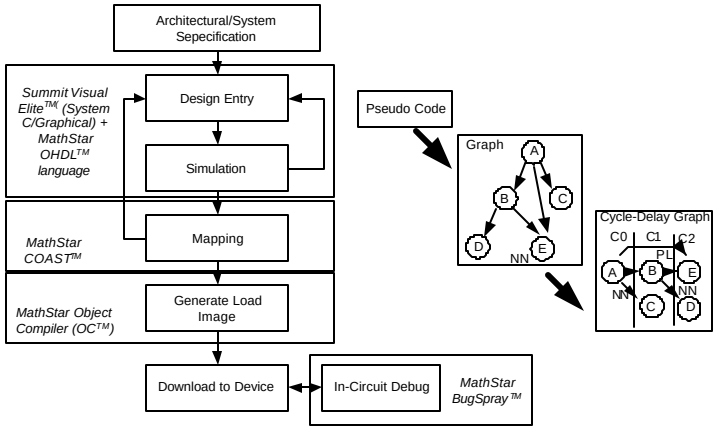

Figure 3: Basic Programming Model

III. Complex FFT

With the mapping as shown in Figure 4, the MathStar FPOA FilterBuilder platform can achieve the performance of $\log_2 N * N/(2*BF) * 6$ cycles for a N-pt FFT, where BF is the number of butterfly tiles available. There are 32 butterfly tiles in the first MathStar FPOA FilterBuilder platform chip. At 1GHz operating frequency, a 1024-point Complex FFT takes 960ns with a non-pipelined low latency implementation.

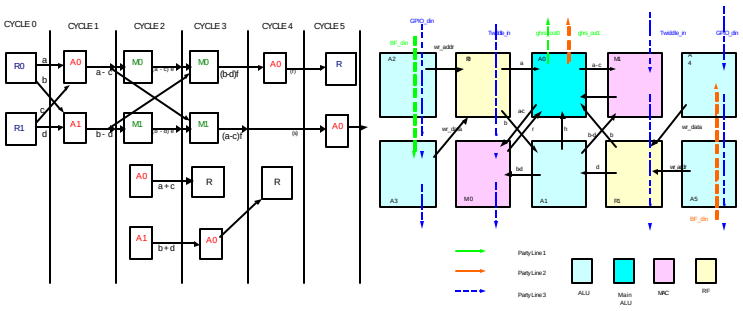

Figure 4: Cycle-delay Graph and Mapping of the Radix-2 Butterfly

IV. Conclusion

MathStar is commercializing a production-grade high-performance re-programmable platform chip (Field Programmable Object Array) with detailed attention to performance, efficiency, and flexibility. The first chip provides a massively parallel processing environment with synchronous interconnect, targeted at high-performance signal processing. There is a high demand in the market today for solutions to support high-performance signal processing applications. MathStar's FPOA is an ideal solution for these types of applications. MathStar's FPOA delivers performance that is an order of magnitude higher than competitive re-programmable computing engines. MathStar's FPOA offers a significant advantage over conventional DSPs, FPGAs and ASICs by delivering a high-performance solution and a radically simplified design-to-production flow. This solution reduces the time-to-market for cost conscious, and technically savvy customers who are seeking to implement an ASIC-scale alternative for high-performance digital signal processing at a startlingly lower cost.