A High Performance Field Programmable Gate Arrays Created by SiGe HBT BiCMOS

Jong-Ru Guo, C. You, M. Chu, K. Zhou, J. Diao, B. Goda*, R. P. Kraft and J. F. McDonald
guoj@rpi.edu
518-2762512
Rensselaer Polytechnic Institute, Troy NY 12180
*United States Military Academy, West Point NY 10096

Field programmable gate arrays (FPGAs) are now widely used for the implementation of digital systems. First introduced by Xilinx, FPGAs have demonstrated their versatility in many fields such as networking and digital signal processing (DSP). However, the relatively low operating frequency of CMOS FPGAs cannot handle the requirements of Gigahertz applications.

In 2000, the first high speed SiGe FPGA utilizing Current Mode Logic (CML) was proposed. The excellent high speed performance that CML allows made it a good candidate for use in high speed FPGA design. However, the large power consumption associated with CML (108mW for the FPGA building block) made the design difficult to scale up. To alleviate this problem, an improved FPGA with shorter propagation delays and less power consumption is now proposed.

Technical progress in bringing SiGe HBT technology to reality has been exceptionally rapid. The IBM SiGe BiCMOS process has evolved over several generations, resulting in the HBT's cutoff frequency approaching 120GHz (for 7HP) and is still increasing; a 210GHz process (8HP) has just been released. Based on the graded Ge alloy base, the Ge content varies linearly across the base to create a built-in electric field that aids the faster movement of minority carriers. This reduces the base transit time to increase its cutoff frequency. SiGe technology offers the speed of the III-V devices with better yield and lower cost. With the excellent high speed performance, the operating frequency of some SiGe applications has reached 40GHz.

CML is the second generation of Emitter Coupled Logic (ECL). The reference current is provided at the bottom of the current tree. By properly steering the current (I_{ref}) flow through the emitter couple pair inputs and the voltage drop resistors, the desired output voltage is achieved. The value of the input differential voltage that fully switches the current to one side is about 200mV. Therefore, most CML circuits operate at an input and output voltage differential larger than 200mV. By following this principle, CML has three different voltage levels as inputs in designs. The ranges of those levels are Level 1: 0 ~ -0.25V, Level 2: -0.95V ~ -1.2V and Level 3: -1.9V ~ -2.15V. The power consumption of the CML is proportional to the power supply voltage and reference current. Thus, to reduce the power consumption, a designer needs to reduce the reference current and power supply voltage.

The SiGe FPGA presented in this paper is based on the Xilinx 6200, and has been developed over several SiGe processes. With the SiGe FPGA, the major problem in the original design is the power wasted by the constant flow of reference current that contributes a significant quantity of static power towards the overall power consumed. A decrease in operating voltage and reference current can help lower the static power, as can modifications to turn off unused CML trees. Both of these techniques have been used in the latest design, yielding significant improvements.

By using the modified CML tree, more input levels can be discarded. The supply voltage is reduced from 4.5 V used in the 5HP SiGe FPGA to 2.2 V used in the 8 HP SiGe FPGAs. At the same time, the reference current is set around the highest fT to bias transistors at their fastest speed. The reference currents used in the 5HP and 7HP SiGe FPGAs are both 0.8mA and 0.7mA is used in the 8HP FPGA. Thus, the overall power consumption is reduced 57.22% from the 5HP generation to the 8HP generation. Though the reduction in power supply voltage has contributed to significant power savings, a multiple power shutdown scheme has been developed to further reduce the power consumption. With these two techniques combined, a reduction of up to 86% over the 5HP design has been achieved.

In order to test the SiGe FPGAs' performance, ring oscillators have been designed. From the measurement and simulation results, the propagation delay of the SiGe FPGA have been greatly reduced from 130ps (5HP) to 42ps (8HP) for a single CLB. Some applications implemented by the SiGe FPGA have been simulated as well, including a 4:1 multiplexer and 1:4 demultiplexer. The simulation results show both circuits can operate at a 10 Gbps transmission rate. A shift register that can run up to 13 GHz has also been simulated.

From the above simulation and measured results, the SiGe FPGA can run in the GHz range while implementing various applications.

Future work:
A larger scale 7HP SiGe FPGA is to be fabricated. It can be used to perform high-speed DSP applications, such as software radar, poly-phase filtering, etc in the GHz range. An ADC is being developed by the same research team as a high speed front end for translating high frequency analog signals into a digital data stream, to be demultiplexed and processed by the SiGe FPGA implementing DSP applications, and then recombining the outputs

With SiGe FPGAs, the operating frequency has been demonstrated to be in the GHz range. Applications implemented by it have been demonstrated and simulated. It can be seen that these devices are viable candidates for performing reconfigurable high-speed calculations.