Radiation Hardened, Ultra Low Power, High Performance Space Computer Leveraging COTS Microelectronics with SEE Mitigation

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The development of computer systems for space applications involves the balancing of three interrelated features: low power, high performance, and high radiation tolerance. Each of these aspects have been addresses separately in the past and solutions have emerged that can meet desired levels of one or two of these features but not all three.

Commercial microprocessors have been able to achieve both low power and high throughput (1500 to 2000 MIPS at 5 to 10 watts), but fail to have useful radiation tolerance. Radiation hardened microprocessors have been able to achieve solid radiation performance (>100 krad(Si), no single event latchup and single event upset better than 1 upset per 1,000 days/device), but only achieve 250 MIPS throughput performance at 5 to 10 watts. Recent characterizations of advanced commercial foundries show that total ionizing dose (TID) and single event latchup (SEL) tolerance of commercial processes have favorable performance trends, making single event upset (SEU) the primary problem preventing the design of a low power, high speed and radiation hardened computer system.

Space Micro Inc. is developing an ultra-low power high performance space computer architecture that highly leverages commercial microprocessor technology. This space computer architecture combines several low power techniques currently used for PDAs and laptop computers, such as dynamic voltage scaling, frequency scaling and software controlled hardware. In addition, Space Micro has developed a unique patent-pending SEU mitigation technique that enables its computers to exceed SEU performance of traditional radiation-hard computers.

Our Proton100k computer is a high-performance radiation-hardened processing solution that meets the challenges of space and satellite harsh environment platforms. By utilizing Space Micro's radiation hardening technologies and expertly selected commercial microelectronics, the Proton100k is able to provide industry superior performance/power/radiation hardness figures. Space Micro's industry leading solutions for single event and total dose radiation effects provide extraordinary performance benefits by removing the traditional barriers to computer design for space and satellite applications. Target performance of the 32-bit Proton100k single board computer (SBC) is 1200MIPS at 350MHz, with a 5W power budget for the microprocessor. This computer will provide SEL immunity greater than 70MeV/mg/cm^2 and SEU bit error rates of less than 1x10^{-5} unrecoverable upsets per day.

This computer is now in fabrication for spaceflight in early 2005. It will be flight qualified on the Air Force Research Labs (AFRL) Rapid Spaceflight Experiment (RSX).

In this application, the Proton100k will act as the Reconfigurable Onboard Processing Experiment (ROPE) and will process camera images for down-linking.

This paper will illustrate our novel technique in mitigating SEU in an advanced class of microprocessors using the Very Long Instruction Word (VLIW) microprocessor architecture. The SEU mitigation technique, termed Time-Triple Modular Redundancy (TTMR™), will be presented along with a software simulation of its SEU mitigation capability as used in the Proton100k computer. The system performance degradation resulting from using TTMR will be analyzed. Electrical simulation data will be presented showing SEU rate improvement for microprocessors using our technique. Finally, radiation test data from both proton and heavy ion testing will be presented to demonstrate the SEU mitigation and resulting error rates.

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