# EMBEDDED SYSTEM FOR BRUSHLESS MOTOR CONTROL IN SPACE APPLICATIONS

*G. C. Caprini, #F. Innocenti, †L. Fanucci, #S. Ricci,
#G. Taraschi, P. Terreni, M. Tonarelli, #L. Tosi

*Galileo Avionica, Campi Bisenzio (FI), Italy
#Cesvit Microelettronica, Prato, Italy
Dept. of Information Engineering, University of Pisa, Pisa, Italy

## INTRODUCTION

This paper presents a Multi Chip Module (MCM) device, named AMBRA (ASIC for BRushless Motor control in space Applications), designed for high performance synchronous brushless motor control in space applications. This kind of motors are used for their simple and robust construction, high power output to weight ratio, low inertia and optimal performances at high and low speed. Typical applications are scan mirror, thrust vector control actuators, fuel valve control actuators, solar array deployment, control moment gyroscopes, high and low RPM applications, light weight applications and low thermal emission applications. Motor control is achieved through a DSP-based fully digital ASIC architecture. This solution provides, with respect to typical mixed analog-digital control systems, higher flexibility, cost reduction and greater radiation robustness.

## ACTIVITY SUMMARY

AMBRA is a MCM system made up of a digital ASIC, two analog to digital converters and a four double channels multiplexer. Figure 1 shows the system block diagram including the required motor control external components: current signal conditioning, position sensor signal conditioning and 3-phase inverter providing the required power levels for the brushless motor. The system acquires two of the three motor currents and relative position transducer signals and it provides PWM (Pulse Width Modulation) signals to drive the 3-phase inverter. The MCM system exchanges data with the external world through a serial communication interface.

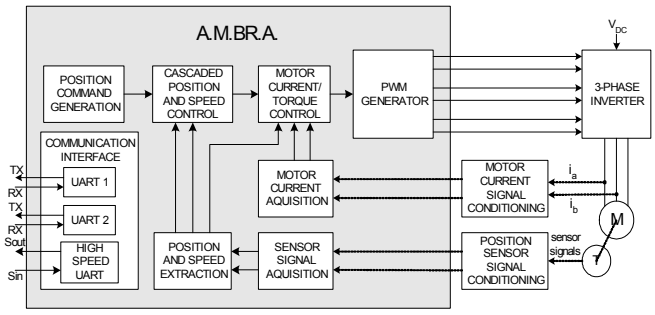


Figure 1 - System block diagram

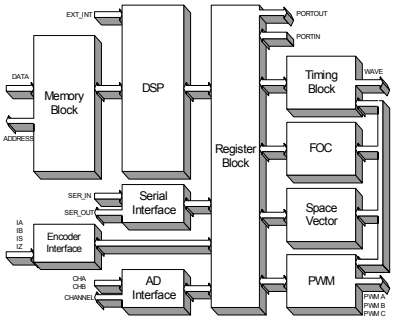


Figure 2 – ASIC architecture

Particularly, AMBRA implements a motor position control based on two nested closed loops. The inner loop is in charge of current and torque controls while the external loop manages the motor position and speed. To this aim, several algorithms have been considered: (i) PID (Proportional Integral Derivative) algorithm to increase dynamic performance in position control; (ii) brushless rotor trajectory generation and (iii) brushless rotor position computation. The latter being the most critical for the overall system performance. These algorithms have been partitioned between hardware and firmware (DSP) implementations according to the required speed performances, their criticality and flexibility (for instance to cope with possible new system requirements).

† Dept. of Information Engineering, University of Pisa, Via G. Caruso, I-56122 PISA – Italy
Phone: +39-050-2217.668 Telefax: +39-050-2217.522 E-mail: l.fanucci@iet.unipi.it

The fully digital ASIC carries out all the functions for brushless motor control generating 3 PWM channels for driving the MOSFET gates of the inverter bridge to reach the final motor position. The latter is input to the ASIC from the external world through a serial interface. Two 12 bit - 10 Msps A/D converters are required to simultaneously sample a couple of homogeneus signals coming from motor current and position sensors .
The ASIC architecture, shown in figure 2, was developed as a trade-off between performance, complexity and flexibility. Besides, to ease ASIC testability, which is of paramount importance in space application, a fully synchronous approach was pursued with the exception of the RAMs (Random Access Memories) control logic operating on both clock edges.
ASIC circuit includes a 16 bit - fixed point DSP macro cell. This DSP is characterized by 10 MIPS computational power which is more than enough with respect to the figure (about 7 MIPS) required to perform all the aforementioned operations, particularly position control and trajectory generation. Two RAM data memories 256x16 and a RAM program memory 2048x16 are included. A FOC (Field Oriented Control) equipment unit implements direct and inverse Clarke & Park transformation for PID calculation. The Serial Interface block in Fig. 2, includes an asynchronous UART in addition to the DSP internal synchronous serial interface. A Timing Unit produces all timing references necessary for AMBRA system operation. The Register Block in Fig. 2 interfaces the DSP core with the rest of the circuit. Space Vector is in charge of controlling the generation of the PWM channels (A, B and C). The Encoder block interfaces an external incremental encoder which is the most used feedback for high performance control systems.
To improve transportability all the hardware blocks have been described in technology-independent VHDL (Very high-speed integrated circuits Hardware Description Language) code. Rotor position elaboration, position PID control function and FOC reference current generation are implemented in firmware by the selected DSP core. To ease maintenance each functionality has been derived ad independent module. A task manager oversees all module operations in a preemptive mode.
Before ASIC foundry run, the overall design has been verified through rapid prototyping on a customarily designed breadboard. The latter features a Xilinx XC2V4000 FPGA, a RS232 interface, two A/D converters, a permanent magnet 3-phase motor with resolver, a 3 phase MOS bridge with relative driver and analog interface modules. The AMBRA circuitry required 33% of the overall FPGA resources (13% due to the DSP core).
Proper test vectors have been developed to verify the functionality of the prototyped system. The same will be applied to the final system featuring the AMBRA ASIC when back from the silicon foundry.

## CONCLUSIONS

After the successful verification of the breadboard prototype, the ASIC design was finalized by means of logic synthesis for the 0.35 µm CMOS Austriamicrosystems technology. The rationale behind this choice is to allow technology access through reduced-price multi-project wafer and at the same time reduce risks in case of technology retargeting to a radiation tolerant technology such as the 0.35 µm CMOS provided by ATMEL (MH1RT).
The final chip resulted, whose layout is shown in Fig. 3, to be PAD limited with an overall area of 19.901 $mm^2$, a clock frequency of 20 MHz and an estimated power consumption of 226.3 mW @ 3.3 V power supply. Fault coverage is greater than 97%. MCM is built on 1.6 mm FR4 substrate with tracks and isolations of 100 µm. System accuracy performances depend on the kind of used resolver. In the prototyping breadboard where we adopted a multi-speed (x1 x8) resolver, the AMBRA position precision amounts to 19 bit.
Summarizing, the main advantages of the presented AMBRA motor control system are: (i) great reduction in the number of devices and consequent size and cost reduction; (ii) increase in the overall reliability due to the fully digital approach; (iii) higher system flexibility and reduced design time/efforts due to a DSP-core based system. Particularly, the latter allows system re-use in many other applications based on actual position sensors (sine/cosine encoder).

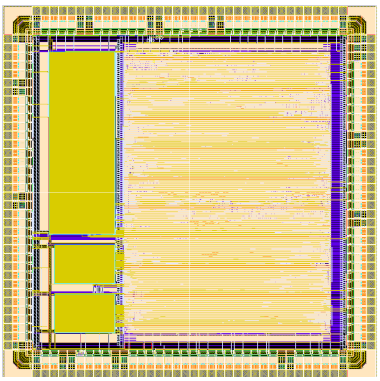

Figure 3 – ASIC layout