An Analytical Approach for Soft Error Rate Estimation of SRAM-Based FPGAs

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Abstract

SRAM-based FPGAs are increasingly becoming more popular in applications where high dependability, low cost, and fast time-to-market are important constraints. However, these devices are more susceptible to single-event upsets (SEUs) compared ASIC designs. The error models of SRAM-based due to SEUs are more complicated than those of ASICs since soft-errors in the configuration memory result in permanent errors in the user application. In this work, we investigate different error models for SRAM-based FPGAs due to soft errors and present analytical soft error rate estimation for these devices.

1. Introduction

Nowadays, FPGAs are widely utilized in many applications such as industrial, spacecraft and embedded applications. They are increasingly used in applications where previously were exclusive territory of ASICs. Electronic designers use FPGA because of its high flexibility in achieving multiple requirements such as high performance, no Non-Refundable-Engineering cost and fast Time-To-Market [Lima01]. It is notable to mention that designers, who preferred ASIC, are now using the mixed FPGA-ASIC solution.

Although SRAM-based FPGAs provides the advantages of low-cost design and fast Time-To-Market, the importance of dependability issues limit their widespread adoption in mission-critical applications [Lima01]. That is, the SRAM-based FPGA technology is sensible to Single Event Upsets (SEUs) [Normand96] that may be induced by charged particles hitting the silicon affecting the logic state of memory elements to be changed. One way to avoid this problem is to use radiation hardened FPGA devices. However, these devices are much more expensive than Commercial-Off-The-Shelf (COTS) FPGAs; thus when cost is a major issue, the COTS devices are affordable [Rebaudengo02]. Another way to avoid the above mentioned problem is to include fault-tolerant mechanisms into the designs implemented by the COTS FPGAs but the proposed approaches [Lima01] [Carmichael99] enforce high area and performance loss. To develop efficient fault-tolerant schemes, designers need accurate estimates of soft error rate to develop appropriate cost/performance error-correction and recovery schemes.

Previous work on error rate estimation [Carmichael99] [Lima01] [Rebaudengo02] [Fuller00] is mainly simulation-based or radiation-based or combination of both of them; hence most of them are inaccurate and time-consuming.

In this work, first we analyze different error models for SRAM-based FPAGs and then employ an analytical approach to estimate the error rate of the entire chip.

2. Error models

The effects of single event upsets (SEU) on digital circuits can be classified in three ways. First, SEUs can cause a transient error in combinational logic parts, which can be propagated and captured in flip-flips. Second, SEUs can change directly contents of memory elements including memory caches, main memories, register files and flip-flops. These errors may be overwritten or corrected using error-detection-and-correction techniques. Third, SEUs can make permanent errors on SRAM-based combinational logic such as SRAM-based FPGAs. In this case, the error will remain unchanged until the new configuration is downloaded on the FPGA.

The first two types are well described in [Antoni00], [Arlat90], [Iyer96], and [Leveugle00], which investigate the circuit behavior by injecting faults into the simulated or emulated model of the design. The fault injection in these techniques implies the alteration of memory elements such as data-path/control-unit registers as well as alteration of available input or output or internal signals. Consequently, simulating or emulating the effect of SEUs in presence of faults can be studied straightforwardly. In this context, the fault model that is normally adopted for mimicking the effects of SEUs is the transient single bit-flip, which corresponds to the inversion of the logic state of a memory bit [Rebaudengo02]. The third type demands much more complex analysis capabilities. The simple bit-flip fault model cannot be fruitfully exploited; this is due to the effects of SEUs in the device configuration memory are indeed not limited to modifications in the design memory elements, but may produce modifications in the interconnections inside a CLB and among routing signals between different CLBs. The work addressing this aspect has been started since a few years ago [Lima01] [Fuller00] [Rebaudengo02]. To better analysis of SEUs on SRAM-based FPGAs, we classify the effect of soft errors due to SEUs as follow:

2.1. Transient-effect errors

These types of errors do not affect SRAM configuration bits but they may affect any other routing signals, user-defined flip-flops and combinational logic.

a. ***An SEU on combinational part inside CLBs*:** an SEU affecting a combination part makes a transient error on logic gates. This may be propagated to the sequential part and make a bit-flip error. As an example, suppose Figure 1 that shows how an SEU makes a bit-flip on a flip-flop. Most errors occurring on combinational logic are masked and they are not reached to the inputs of the flip-flops. Also, as an SEU is propagated through logic gates, it is more probably to be attenuated by logic gates due to electrical properties of the gates. Even if an error is propagated through all logic gates and reaches to an input of a flip-flop, it may not be ready at appropriate latching-window of flip-flops.

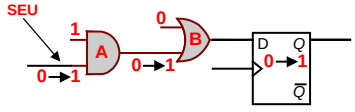

Figure 1: An SEU affects one of inputs of the AND gate and makes a bit-flip error

b. ***An SEU on routing signals*:** an SEU may cause a transient error on routing signals inside a CLB or between two CLBs. This can also be propagated and captured by flip-flops if it reaches in an appropriate latching-window.

c. ***A bit-flip on user-defined flip-flops and memory elements*:** an SEU may directly affect the contents of flip-flops and memory

elements. The flip-flop will remain erroneous until it is rewritten with another data or it is corrected by appropriate error detecting and correcting techniques.

2.2. Permanent-effect errors

These types of errors make permanent effects until the configuration bits re-downloaded into the FPGA.

a. ***A bit-flip on line-segment configuration bits*:** There are a lot of vulnerable routing configuration bits in SRAM-based FPGAs. An SEU changing a configuration routing bit causes a stuck-open, stuck-closed or bridging error (wired-or, wired-and) as shown in Figure 2. Typically almost 80% of transistors in an FPGA are used in the routing network and therefore the effect on routing signals comprises a major part of all of SEUs. An erroneous routing signal may be routes inter CLBs or intra CLB. Moreover, inter CLBs routing signals include switch matrices and line segments. Also, line segments consist single-length lines, hex lines and long-lines. We classify erroneous routing signals because their impact may differ significantly. For example, an erroneous long-line signal impacts more likely the whole system than an erroneous single-length line.

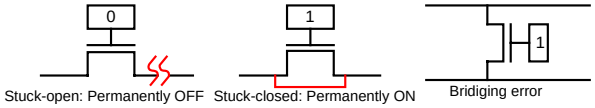

Figure 2: An impact of SEU on routing signals

b. ***A bit-flip on switch-matrix configuration bits*:** A switch-matrix consists of a number of Programmable Interconnect Points (PIPs). Each PIP is pass transistor or series of pass transistors. PIPs error models are stuck-open, stuck-closed, and bridging errors. A typical switch matrix is shown in Figure 3.

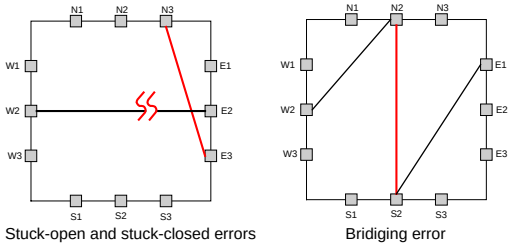

Figure 3: A typical 3x3 switch matrix

c. ***A bit-flip on LUT configuration bits*:** This causes stuck-at fault in combinational logic if it is not x-care bit and consequently changes the functionality of the LUT logic. In this case, the failure probability of the LUT equals the activation probability (signal probability) times the propagation probability.

d. ***A bit-flip on MUX selector configuration bits*:** An error on MUX selector changes the functionality of CLB

e. ***A bit-flip on IOB configuration bits*:** This may cause a serious system failure because it may change the system output paths.

f. ***A bit-flip on TBUF and OBUF*:** This also may have unrecoverable errors in the system.

Every group has its own error behavior. In this work, we model the effects of each group and then compute the soft error rate of a typical FPGA.

3. Error rate estimation

Our framework for error rate estimation is based on some efficient algorithms to traverse the entire circuits from error sites to the system outputs to compute the system failure rate in the polynomial time. We use the signal probabilities of all nodes in the combinational part and then compute error propagation probabilities based on the topological structure of the circuit. It is notable that signal probability calculation is widely used for accurate estimation of signal activity and power dissipation of circuits. By reusing these results from previous design steps, the complexity of our approach will not increase. As an example, consider Figure 4, which shows a typical path between an error site to a primary output.

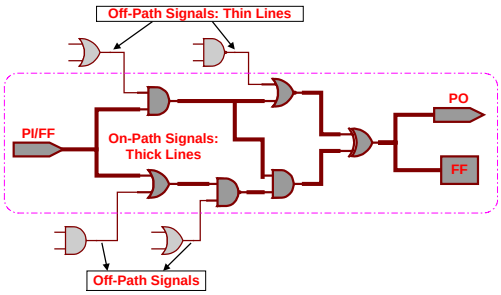

Figure 4: A typical path between a faulty input/flip-flop to a primary output/flip-flop

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