DESIGN OF FAST AND EFFICIENT HYBRID-FPGAs FOR NUMERICALLY INTENSIVE APPLICATIONS IN FLUID DYNAMICS AND IMAGE/VIDEO PROCESSING

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Computationally intensive applications such as numerical simulations in Computational Fluid Dynamics, video and image processing involve modules solving sets of equations or tasks which have common computation features performed iteratively. These domains are known to have a high degree of relevance to military applications. Several researchers have shown that they are well suited for parallel processor architectures. FPGAs offer large amounts of on-chip parallel units, but suffer from drawbacks of being application agnostic by loss of clock cycles in redundant reconfigurations, generic routing and poor memory architectures. These factors have lead us into exploring application specific reconfigurable architecture design space. This paper focuses on extraction of core clusters in Control Data Flow Graphs (CDFGs) of multimedia and fluid dynamics applications followed by designing the architecture to embed them in Hybrid-FPGA environments. Proposed FPGA architecture will involve LUT regions, ASIC regions and possibly VPGA regions. Clusters implemented as ASICs on non-reconfigurable area are recurring computation patterns obtained through common sub-graph analysis between basic blocks within and across routines. After removing the common sub-graphs from the CDFG, remaining parts of each basic block are then implemented on LUT based reconfigurable area. A Packing mechanism designed to improve the routing architecture by reducing the switching requirements by 12-20% in configurable logic has been proposed. Mechanism uses live-in live-out variable analysis and scheduling information of CDFGs in its cost function in addition to routability and timing driven cost metrics defined by other researchers. We have conducted experiments on complex routines from the target applications. Map/synthesis reports based on Xilinx architectures were obtained. Results show that partial reconfiguration with the use of computation cores embedded in a sea of LUTs offer potential for massive savings in gate density. In addition to that, by eliminating the need for unnecessary and redundant sub-circuit pattern configurations, switching requirements in configurable area is reduced due to localization of global connections.