SX-A/RT54SX-S SSO Preliminary Results
Publication Motivations

- To address some of the concerns expressed by some customers prior to full report completion.

- To assist customers with the currently available data to make assessment of their chip and board designs.

- Currently more data are being collected.
  - The current guidelines will be substantiated with more data.
Full Characterization Plan includes a large number of parameters, SSO is one of them.

SSO Characterization Status

- Available data are on 3.3V IO STD and based on SX-A/PQ208 and RT54SX-S/CQ208.

- General Guidelines pending on completion of data collection.
Parameters Considered for SSO

- Peak / Valley Voltages (Volp / Volv)
- Settling Time
- Peak Pulse Width (PPW)
- Minimum Switching Window (MSW)
- Slew Rate
- Output Capacitance
- Package
- IO Std (including voltage)
- IO Type (Quiet Output or Clock)
Content

- Test Setup
- Test Operating Conditions
- Current Status
- Sample Output
- Results
- Summary
Test Setup

R_L = 500
C_L = 50pF
per MilStd Test Method 3024
Definitions

Switching Output 1

Switching Window

Switching Output N

Quiet Output

VOLP

VII_{MAX}

GND (0V)

VOLV

PPW

Settling Time

Definitions

GND (0V)

VIL

MAX

VOLP

VOLV
Test Operating Conditions

- **High Slew Data Based on MIL-STD 883E Method 3024:**
  - Temperature = 25°C, Core Voltage 2.5V, IO Voltage 3.3V
  - Load: $R_L=500\,\Omega$ in parallel with $C_L=50\,\text{pF}$
  - The MIL-STD load requirement might be conservative for most of the designs.
    - Additional measurements for other loads on-going

- **Low Slew Falling Edge Data Based on:**
  - Temperature = 25°C, Core Voltage 2.5V, IO Voltage 3.3V
  - Based on socketed part with no load.
  - Measurements for soldered part with load are on-going.
Test Operating Conditions

- All outputs switch within a 1.2nS window
  - This is a realistic window, but typical windows are usually larger.

- Measurements are done on the following pins (*):
  - Quiet Output : pin #138
  - Switching Outputs : pins #111 to #162

(* ) Please refer to the RT54SX-S Data Sheet for more information
Current Status

Initial Results Collected for
- High Slew Rising and Falling edge data on RT54SX-S/CQ208
- Low Slew Falling edge data based on SX-A/PQ208 (* )
- 3.3V IO Standards
  - 5.0V IO Standards measurements on-going

Data Provided
- Volp (peak) and Volv (valley) of the Quiet Output
- Peak Pulse Width (PPW) and Settling Time
- SSO Effect on the HCLK Clock Buffer
- SSO Effect on the CLKA/CLKB Clock Buffer

( * ) Socketed with no load
Results

For Up To 40 SSOs:

- Results are based on 3.3V IO configuration
  - 5.0V standards measurements on-going

- Results remain flat for 20 SSOs and above

- Low-Slew Configuration:
  - Falling Edge data measured on an aggressive SSO environment:
    - SX-A/PQ208, socketed, with no load
  - Quiet Output Volp = 0.85V
  - Quiet Output Max PPW < 200pS
Results

For Up To 40 SSOs:

- **High Slew Configuration:**
  - Quiet Output Volp < 2V
  - Width at 1.5V < 0.6nS
  - Width at LVTTL VILmax (0.8V) < 2nS

- **Reminder:** CMOS standard has higher VIH limit than TTL:
  - 5V CMOS VIHmin = 0.7*VCC / VILmax = 0.3*VCC
  - TTL/LVTTL VIHmin = 2.0V / VILmax = 0.8V
Results

For Up To 40 SSOs:

- No Impact on the HCLK Network

- RCLK Analysis:
  - Current data are based on inadequate setup (socketed part)
  - Current data show no glitch for up to 16 SSOs
  - Data collection for soldered parts are on-going
Next Steps

- **Initial SSO Analysis:**
  - 5V IO Standards
  - Output Load Effect
    - 500Ω/50pF, 5KΩ/50pF, 10KΩ/50pF
    - 500Ω/20pF, 500Ω/100pF
  - Actel SX-A/RT54SX-S Initial SSO Guideline

- **Extended SSO Analysis:**
  - SXS Low-Slew Volp, Volv, PPW, and Settling Time
  - SSO Effect on CLKA/CLKB with soldered part
  - SSO Effect on the QCLK Clock Buffer
  - Expanding the Minimum Switching Window
  - Actel SX-A/RT54SX-S Extended SSO Guideline