

<b>NOTICE OF REVISION (NOR)</b>		1. DATE (YYMMDD) 96-10-04	Form Approved OMB No. 0704-0188
THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.			
Public reporting burden for this collection is estimated to average 2 hours per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503. PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSES. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/ PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.		2. PROCURING ACTIVITY NO.	
		3. DODAAC	
4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code) Defense Supply Center Columbus 3990 Broad Street Columbus, OH 43216-5000	5. CAGE CODE 67268	6. NOR NO. 5962-R003-97
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE 67268	8. DOCUMENT NO. <b>5962-89713</b>
9. TITLE OF DOCUMENT  MICROCIRCUIT, MEMORY, DIGITAL CMOS, PROGRAMMABLE LOGIC CELL ARRAY, MONOLITHIC SILICON		10. REVISION LETTER	
		a. CURRENT D	b. NEW E
11. ECP NO.			
12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES All			
13. DESCRIPTION OF REVISION  Sheet 1: Revisions ltr column; add "E". Revisions description column; add "Changes in accordance with NOR 5962-R003-97". Revisions date column; add "96-10-04". Rev status above sheet numbers 1 and 16, delete "D", and add "E". Revision level block; delete "D", and add "E".  Sheet 16: Table I, footnote 3/ Delete the last sentence of this footnote and replace it with the following: "Characterization data is taken initially and after any design or process change which may affect this parameter." Revision level block; delete "D", and add "E".			
14. THIS SECTION FOR GOVERNMENT USE ONLY			
a. (X one)	X	(1) Existing document supplemented by the NOR may be used in manufacture.	
		(2) Revised document must be received before manufacturer may incorporate this change.	
		(3) Custodian of master document shall make above revision and furnish revised document.	
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT  DSCC-VAS		c. TYPED NAME (First, Middle Initial, Last)  Ray Monnin	
d. TITLE  Microelectronics Team Chief	e. SIGNATURE  Ray Monnin		f. DATE SIGNED (YYMMDD) 96-10-04
15a. ACTIVITY ACCOMPLISHING REVISION  DSCC-VAS	b. REVISION COMPLETED (Signature)  Kenneth S. Rice		c. DATE SIGNED (YYMMDD) 96-10-04

<b>NOTICE OF REVISION (NOR)</b>		1. DATE (YYMMDD) 95-10-05	Form Approved OMB No. 0704-0188
THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.			
Public reporting burden for this collection is estimated to average 2 hours per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503. PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSES. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.			2. PROCURING ACTIVITY NO.
			3. DODAAC
4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code) Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5765	5. CAGE CODE 67268	6. NOR NO. 5962-R199-95
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE 67268	8. DOCUMENT NO. <b>5962-89713</b>
9. TITLE OF DOCUMENT MICROCIRCUIT, MEMORY, DIGITAL CMOS, 4200 GATE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON		10. REVISION LETTER	
		a. CURRENT C	b. NEW D
11. ECP NO. N/A			
12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES All			
13. DESCRIPTION OF REVISION			
<p>Sheet 1: Revisions ltr column; add "D". Revisions description column; add "Changes in accordance with NOR 5962-R199-95". Revisions date column; add "95-10-05". Revision level block; change from "C" to "D". Rev status of sheets; for sheet 1, change from "C" to "D". For sheet 8, change from "B" to "D". For sheet 16, change from "B" to "D".</p> <p>Sheet 8: For the three capacitance tests; "Input capacitance except XTL1 and XTL2" change the max limit from 10 pF to 16 pF., "Input capacitance XTL1 and XTL2" change the max limit from 15 pF to 20 pF., "Output capacitance" change max limit from 10 pF to 16 pF. Revision level block; change from "B" to "D".</p> <p>Sheet 16: For footnote 1/, after the last line; "5 inputs at 10 Mhz"; add double blank lines and continue the note with the following: "Excessive supply current can occur as a result of internal contention during the initial phase of a reconfiguration following a short interruption of Vcc. To avoid this excessive current, monitor the dropping of Vcc and immediately initiate a reconfiguration, but hold RESET active. This clears the internal configuration register in less than a millisecond, and avoids all later contentions." Revision level block; change from "B" to "D".</p>			
14. THIS SECTION FOR GOVERNMENT USE ONLY			
a. (X one)	X	(1) Existing document supplemented by the NOR may be used in manufacture.	
		(2) Revised document must be received before manufacturer may incorporate this change.	
		(3) Custodian of master document shall make above revision and furnish revised document.	
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ELDS		c. TYPED NAME (First, Middle Initial, Last) Michael A. Frye	
d. TITLE Microelectronics Branch Chief	e. SIGNATURE Michael A. Frye		f. DATE SIGNED (YYMMDD) 95-10-05
15a. ACTIVITY ACCOMPLISHING REVISION DESC-ELDS	b. REVISION COMPLETED (Signature) Kenneth S. Rice		c. DATE SIGNED (YYMMDD) 95-10-05

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Redrawn with changes. Converted drawing to one part-one part number SMD format. Added package, outline letters U and T. Added devices 03 and 04	93-09-14	M. A. Frye
B	Added case outline N. Made format changes, editorial changes throughout.	94-02-04	M. A. Frye
C	Added case outline M, 9, and 8. Editorial changes throughout.	94-06-06	M. A. Frye

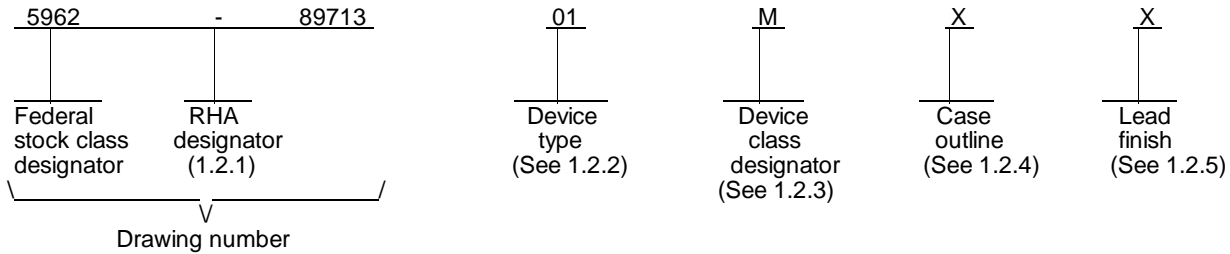
REV	C	C	C																	
SHEET	35	36	37																	
REV	B	B	B	B	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS OF SHEETS				REV			C	C	C	B	B	B	B	B	B	B	B	B	B	B
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

<p align="center"><b>STANDARDIZED MILITARY DRAWING</b></p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	PMIC N/A	PREPARED BY Kenneth Rice	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		
		CHECKED BY Rajesh Pithadia			
		APPROVED BY Mike Frye			
		DRAWING APPROVAL DATE 92-07-28	SIZE <b>A</b>	CAGE CODE <b>67268</b>	<b>5962-89713</b>
		REVISION LEVEL C	SHEET 1 OF 37		

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Toggle Speed</u>
01	3042-50	12x12 4200 gate programmable array	50 MHz
02	3042-70	12x12 4200 gate programmable array	70 MHz
03	3042-100	12x12 4200 gate programmable array	100 MHz
04	3042-125	12x12 4200 gate programmable array	125 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outlines shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CMGA15-PN	84 1/	Pin grid array package
Y	See figure 1	100	Quad flat package
Z	CMGA6-PN	132 2/	Pin grid array package
U	CMGA3-PN	84 1/	Pin grid array package
T	CQCC1-F100	100	Unformed-lead chip carrier 3/
N	See figure 1	100	Quad flat package
M	See figure 1	100	Quad flat package
9	See figure 1	100	Quad flat package
8	See figure 1	100	Quad flat package

1/ 84 = actual number of pins used, not maximum listed in MIL-STD-1835

2/ 132 = actual number of pins used, not maximum listed in MIL-STD-1835

3/ Pin 1 is the middle pin on the side with center justified identifier mark. Mark may be a notch, dot, or triangle.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	SIZE <b>A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET <b>4</b>

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 3/

Supply voltage range to ground potential ( $V_{CC}$ )	.....	-0.5 V dc to +7.0 V dc
DC input voltage range	.....	-0.5 V dc to $V_{CC}$ +0.5 V dc
Voltage applied to three-state output ( $V_{TS}$ )	.....	-0.5 V dc to $V_{CC}$ +0.5 V dc
Lead temperature (soldering, 10 seconds)	.....	+260° C
Thermal resistance, junction-to-case ( $\Theta_{JC}$ ):		
Case outline X, Z, U, and T	.....	See MIL-STD-1835
Case outlines Y, N, M, 9, and 8	.....	10° C/W 4/
Junction temperature ( $T_J$ )	.....	+150° C 5/
Storage temperature range	.....	-65° C to +150° C

1.4 Recommended operating conditions. 6/

Case operating temperature Range ( $T_C$ )	.....	-55° C to +125° C
Supply voltage relative to ground ( $V_{CC}$ )	.....	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND) or ( $V_{SS}$ )	.....	0 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests in accordance with MIL-I-38535	.....	95 percent
----------------------------------------------------------------------------------------	-------	------------

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.  
 4/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.  
 5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.  
 6/ All voltage values in this drawing are with respect to  $V_{SS}$ .

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	SIZE <b>A</b>		<b>5962-89713</b>
		REVISION LEVEL <b>C</b>	SHEET <b>5</b>

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with figure 1 and 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic block diagram. The logic block diagram shall be as specified in figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		<b>REVISION LEVEL C</b>	<b>SHEET 6</b>

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.8.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.8.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-I-38535, appendix A).

3.11 Operational notes. Additional information shall be provided by the device manufacturer (see 6.7 herein).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M.

- a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
- c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		<b>REVISION LEVEL C</b>	<b>SHEET 7</b>

- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M subgroups 7, 8A and 8B tests shall consist of verifying functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available upon request. For device classes Q and V subgroups 7, 8A and 8B shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.
- e. Subgroup 4 ( $C_{IN}$  and  $C_{OUT}$  measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b.  $T_A = +125^\circ C$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		<b>REVISION LEVEL C</b>	<b>SHEET 8</b>



TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V, -55° C ≤ T <sub>C</sub> ≤ +125° C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IH</sub> = 0.8 V, I <sub>OH</sub> = -4.0 mA, V <sub>IH</sub> = 2.0 V	1,2,3	All	3.7		V
		V <sub>CC</sub> = 4.5 V and 5.5 V, V <sub>IH</sub> = 0.9 V and 1.1 V, V <sub>IH</sub> = 3.15 V and 3.85 V, I <sub>OH</sub> = -4.0 mA					
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 5.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2.0 V	1,2,3	All		0.4	V
		V <sub>CC</sub> = 4.5 V and 5.5 V, V <sub>IH</sub> = 0.9 V and 1.1 V, V <sub>IH</sub> = 3.15 V and 3.85 V, I <sub>OL</sub> = 4.0 mA					
Operating power supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V 1/	1,2,3	01		245	mA
				02		250	
				03		260	
				04		270	
Quiescent power supply current	I <sub>CCO</sub>	CMOS inputs, V <sub>CC</sub> = V <sub>IN</sub> = 5.5 V	1,2,3	All		2.0	mA
Quiescent power supply current	I <sub>CCO</sub>	TTL inputs, V <sub>CC</sub> = V <sub>IN</sub> = 5.5 V	1,2,3	All		15	mA
Power-down supply current	I <sub>CCPD</sub>	PWRDWN = 0 V, V <sub>CC</sub> = V <sub>IN</sub> = 5.5 V	1,2,3	All		1.15	mA
Input leakage current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V and 5.5 V	1,2,3	All	-20	20	μA
Output leakage current	I <sub>OL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V and 5.5 V	1,2,3	All	-20	20	μA
Horizontal long line, pull-up current	I <sub>RLL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V and 5.5 V	1,2,3	All		2.5	mA

See footnotes at end of table.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 9

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V -55° C ≤ T <sub>C</sub> ≤ +125° C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V <sub>IHT</sub>	TTL inputs	1,2,3	All	2.0		V
Low level input voltage	V <sub>ILT</sub>	TTL inputs	1,2,3	All		0.8	V
High level input voltage	V <sub>IHC</sub>	CMOS inputs	1,2,3	All	0.7 V <sub>CC</sub>		V
Low level input voltage	V <sub>ILC</sub>	CMOS inputs	1,2,3	All		0.2 V <sub>CC</sub>	V
Power down (PWRDWN) voltage $\bar{2}$	V <sub>PD</sub>		1,2,3	All	3.5		V
Input capacitance except XTL1 and XTL2	C <sub>IN</sub>	See 4.4.1e	4	All		10	pF
Input capacitance XTL1 and XTL2	C <sub>IN</sub>	See 4.4.1e	4	All		15	pF
Output capacitance	C <sub>OUT</sub>	See 4.4.1e	4	All		10	pF
Functional test		See 4.4.1c	7,8A,8B	All			
Interconnect + t <sub>PID</sub> + 12(t <sub>ILO</sub> ) + t <sub>OP</sub>	t <sub>B1</sub>	Measured on 12 columns	9,10,11	01		192	ns
				02		122	
				03		98	
				04		78	
t <sub>CKO</sub> + t <sub>ICK</sub> + t <sub>CKI</sub> + interconnect	t <sub>B2</sub>	Tested on all CLB's	9,10,11	01		32	ns
				02		21	
				03		18	
				04		15	

See footnotes at end of table.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 10

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V -55° C ≤ T <sub>C</sub> ≤ +125° C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Interconnect + t <sub>CKO</sub> + t <sub>QLO</sub> + t <sub>ILO</sub> + t <sub>DICK</sub>	t <sub>B3</sub>	Tested on all CLB's	9,10,11	01		53	ns
				02		34	
				03		26	
				04		22	
t <sub>ILO</sub> + t <sub>ECCK</sub> + interconnect	t <sub>B4</sub>	Tested on all CLB's	9,10,11	01		35	ns
				02		23	
				03		19	
				04		17	
t <sub>OKPO</sub> + t <sub>OPS</sub> - t <sub>OPF</sub> + t <sub>PICK</sub>	t <sub>B5</sub>	Tested on all CLB's	9,10,11	01		73	ns
				02		53	
				03		44	
				04		40	
Interconnect + t <sub>CKO</sub> + t <sub>QLO</sub> + t <sub>PUS</sub> + t <sub>ICK</sub>	t <sub>B6</sub>	One long line pull-up	9,10,11	01		73	ns
				02		48	
				03		34	
				04		30	
Interconnect + t <sub>CKO</sub> + t <sub>QLO</sub> + t <sub>PUS</sub> + t <sub>ICK</sub>	t <sub>B7</sub>	Other long line pull-up	9,10,11	01		83	ns
				02		55	
				03		49	
				04		40.5	

See footnotes at end of table.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 11

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V -55° C ≤ T <sub>C</sub> ≤ +125° C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Interconnect + t <sub>CKO</sub> + t <sub>QLO</sub> + t <sub>IO</sub> + t <sub>ICK</sub>	t <sub>B8</sub>	No pull-up, lower long lines	9,10,11	01		47	ns
				02		31	
				03		25	
				04		22	
Interconnect + t <sub>CKO</sub> + t <sub>QLO</sub> + t <sub>ICK</sub> + t <sub>IO</sub>	t <sub>B9</sub>	No pull-up, upper long lines	9,10,11	01		57	ns
				02		38	
				03		32	
				04		28	
Logic input to output (combinatorial)	t <sub>ILO</sub>	See figure 4	3/	01		14	ns
				02		9.0	
				03		7	
				04		5.5	
Reset input to output	t <sub>RIO</sub>		3/	01		15	ns
				02		8.0	
				03		7	
				04		6	
Reset direct width	t <sub>RPW</sub>		3/	01	12		ns
				02	8.0		
				03	7		
				04	6		

See footnotes at end of table.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 12

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V -55° C ≤ T <sub>C</sub> ≤ +125° C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Master reset pin to CLB output (X and Y)	t <sub>MRQ</sub>	See figure 4	3/	01		30	ns
				02		24	
				03		19	
				04		17	
K clock input to CLB output	t <sub>CKO</sub>		3/	01		12	ns
				02		8	
				03		6	
				04		5	
Clock K to the outputs X or Y when Q is return through the function generators to drive X or Y	t <sub>QLO</sub>		3/	01		25	ns
				02		13	
				03		10	
				04		8	
K clock logic-input setup	t <sub>ICK</sub>		3/	01	12		ns
				02	8.0		
				03	7		
				04	5.5		
K clock logic-input hold	t <sub>CKI</sub>		3/	All	1.0		ns
Logic input setup to K clock	t <sub>DICK</sub>		3/	01	8.0		ns
				02	5.0		
				03	4		
				04	3		

See footnotes at end of table.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 13

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V -55° C ≤ T <sub>C</sub> ≤ +125° C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic input hold from K clock	t <sub>CKDI</sub>	See figure 4	3/	01	6.0		ns
				02	4.0		
				03	2		
				04	1.5		
Logic input setup to enable clock	t <sub>ECCK</sub>		3/	01	10		ns
				02	7.0		
				03	5		
				04	4.5		
Logic input hold to enable clock	t <sub>CKEC</sub>		3/	All	2.5		ns
Clock (high) 4/	t <sub>CH</sub>		3/	01	9.0		ns
				02	5.0		
				03	4		
				04	3		
Clock (low) 4/	t <sub>CL</sub>		3/	01	9.0		ns
				02	5.0		
				03	4		
				04	3		
Pad (package pin) to input direct	t <sub>PID</sub>		3/	01		10.0	ns
				02		6.0	
				03		4	
				04		3	
Fast (CMOS only) input pad through clock buffer to any CLB or IOB clock input	t <sub>PGCC</sub>		3/	01		8.5	ns
			02,03,				
			04		6.5		

See footnotes at end of table.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
A

5962-89713

REVISION LEVEL  
C

SHEET  
14

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V -55° C ≤ T <sub>C</sub> ≤ +125° C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
I/O clock to I/O RI input (FF)	t <sub>IKRI</sub>	See figure 4	3/	01		11	ns
				02		5.5	
				03		4	
				04		3	
I/O clock to pad-input setup	t <sub>PICK</sub>		3/	01	30		ns
				02	20		
				03	17		
				04	16		
I/O clock to pad-input hold	t <sub>IKPI</sub>		3/	All	0		ns
I/O clock to pad (fast)	t <sub>OKPO</sub>		3/	01		18	ns
				02		13	
				03		10	
				04		9	
I/O clock to pad-output setup	t <sub>OOK</sub>		3/	01	15		ns
				02	10		
				03	9		
				04	8		
I/O clock to pad-output hold	t <sub>OKO</sub>		3/	All	0		ns
I/O clock (high) 5/	t <sub>IOH</sub>		3/	01	9.0		ns
				02	5.0		
				03	4		
				04	3		

See footnotes at end of table.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
A

5962-89713

REVISION LEVEL  
C

SHEET  
15

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V -55° C ≤ T <sub>C</sub> ≤ +125° C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
I/O clock (low) 5/	t <sub>IOL</sub>	See figure 4	3/	01	9.0		ns
				02	5.0		
				03	4		
				04	3		
Output (enabled fast) to pad	t <sub>OPF</sub>		3/	01		15	ns
				02		9.0	
				03		6	
				04		5	
Output (enabled slow) to pad	t <sub>OPS</sub>		3/	01		40	ns
				02		33	
				03		24	
				04		20	
Three-state to pad begin high impedance (fast)	t <sub>TSHZ</sub>		3/	01		14	ns
				02		12	
				03		10	
				04		9	
Three-state to pad end high impedance (fast)	t <sub>TSON</sub>		3/	01		20	ns
				02		14	
				03		12	
				04		11	
Master RESET to input RI	t <sub>RRI</sub>		3/	01		37	ns
				02		27	
				03,04		24	

See footnotes at end of table.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		<b>REVISION LEVEL C</b>	<b>SHEET 16</b>



TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V -55° C ≤ T <sub>C</sub> ≤ +125° C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Master RESET to output (FF)	t <sub>RPO</sub>	See figure 4	3/	01		55	ns
				02		43	
				03		33	
				04		29	
Bidirectional buffer delay	t <sub>BIDI</sub>		3/	01		4.0	ns
				02		2.0	
				03		1.8	
				04		1.7	
TBUF data input to output	t <sub>IO</sub>		3/	01		8.0	ns
				02		5.0	
				03		4.7	
				04		4.5	
TBUF three-state to output active and valid (single pull-up) double pull-up	t <sub>ON</sub>		3/	All		15	ns
						16	
TBUF three-state to output inactive (single pull-up)	t <sub>PUS</sub>		3/	01		42	ns
				02		36	
				03		22	
				04		17	
TBUF three-state to output inactive (pair of pull-ups)	t <sub>PUF</sub>		3/	01		22	ns
				02		17	
				03		15	
				04		12	

See footnotes at end of table.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
A

5962-89713

REVISION LEVEL  
C

SHEET  
17

TABLE I. Electrical performance characteristics - Continued.

- 1/ Tested initially and after any design or process change that may affect this parameter and guaranteed to the limits specified in table I with the following conditions:
  - Global clock at 16 MHz for device type 01 and 25 MHz for device types 02, 03, and 04.
  - 10 outputs at 5 MHz
  - 25 outputs at 1 MHz
  - Alternate clock at 10 MHz
  - 50 configurable logic blocks (CLB) at 5 MHz
  - 75 CLBs at 1 MHz
  - 15 horizontal long lines at 5 MHz
  - 20 vertical long lines at 1 MHz
  - 25 inputs at 5 MHz
  - 5 inputs at 10 MHz
- 2/ PRWDWN transitions must occur during operational  $V_{CC}$  levels.
- 3/ Parameter is not directly tested. Devices are first 100 percent functionally tested. Benchmark patterns ( $t_{B1-9}$ ) are then used to determine the compliance of this parameter. Characterization data are taken at initial device testing, prior to the introduction of significant changes, and at least twice yearly to monitor correlation between benchmark patterns and this parameter (class M only).
- 4/ Minimum CLOCK widths for the auxiliary buffer are 1.25 times the  $t_{CH}$  and  $t_{CL}$ .
- 5/ These parameters are for clock pulses internal to the chip. Externally applied clock, increases value by 20 percent.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

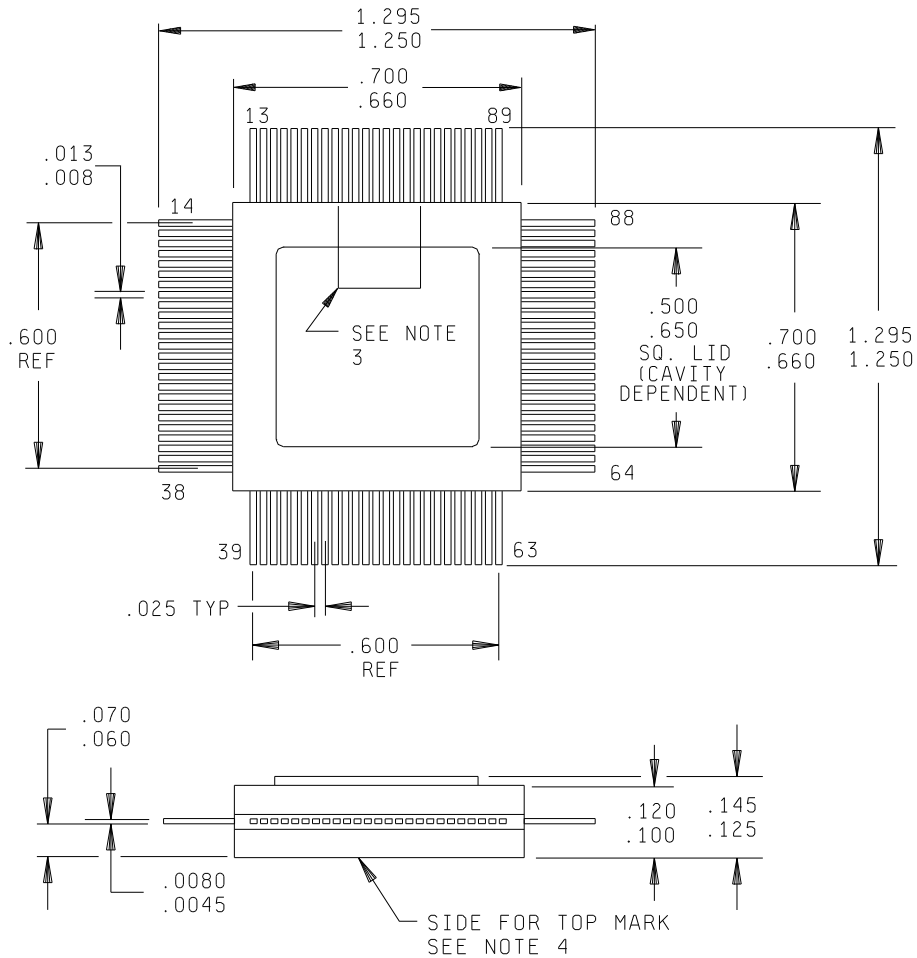
4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ C \pm 5^\circ C$ , after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 18

Case Y



Inches	mm	Inches	mm
.0045	0.114	.125	3.18
.008	0.20	.145	3.68
.013	0.33	.500	12.70
.025	0.64	.600	15.24
.060	1.52	.650	16.51
.070	1.78	.660	16.76
.100	2.54	.700	17.78
.120	3.05	1.250	31.75
		1.295	32.89

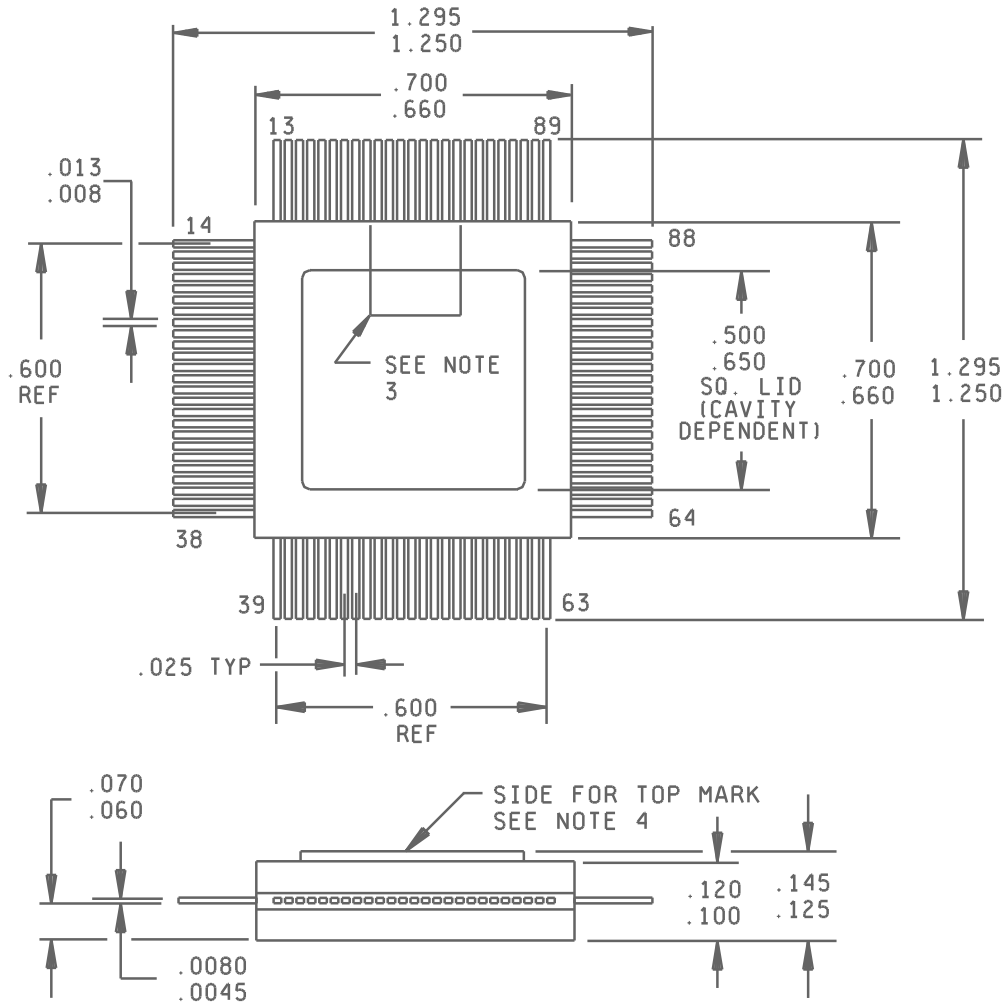
NOTES:

1. Dimensions are in inches.
2. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
3. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. May be a notch, dot, or triangle.
4. Top side mark location, product mark is located on the nonlid side of package; i.e., lid side facing down. When mounted in this position, the pin out is clockwise.

FIGURE 1. Case outline.

<p><b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b></p>	<p>SIZE <b>A</b></p>		<p><b>5962-89713</b></p>
		<p>REVISION LEVEL C</p>	<p>SHEET <b>19</b></p>

Case N



Inches	mm	Inches	mm
.0045	0.114	.125	3.18
.008	0.20	.145	3.68
.013	0.33	.500	12.70
.025	0.64	.600	15.24
.060	1.52	.650	16.51
.070	1.78	.660	16.76
.100	2.54	.700	17.78
.120	3.05	1.250	31.75
		1.295	32.89

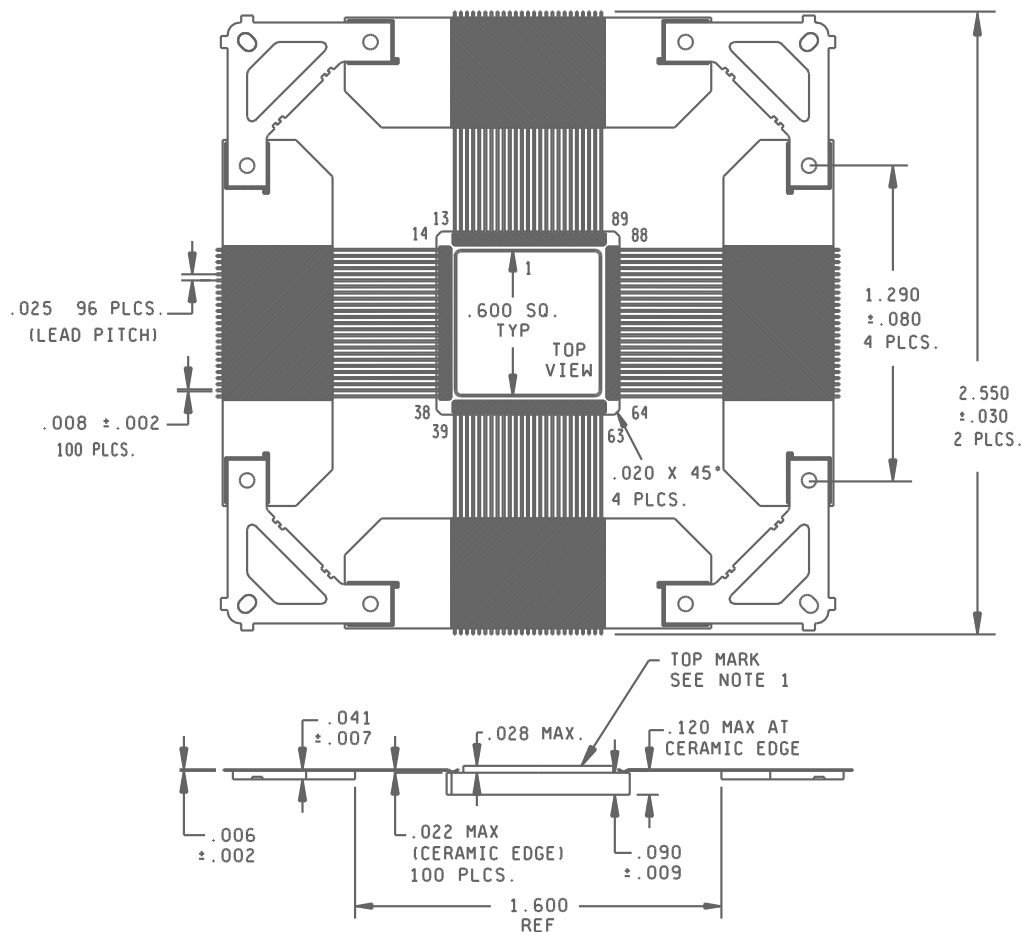
NOTES:

1. Dimensions are in inches.
2. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
3. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. May be a notch, dot, or triangle.
4. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up.  
When mounted in this position, the pin out is counterclockwise

FIGURE 1. Case outline - Continued.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 20

Case M



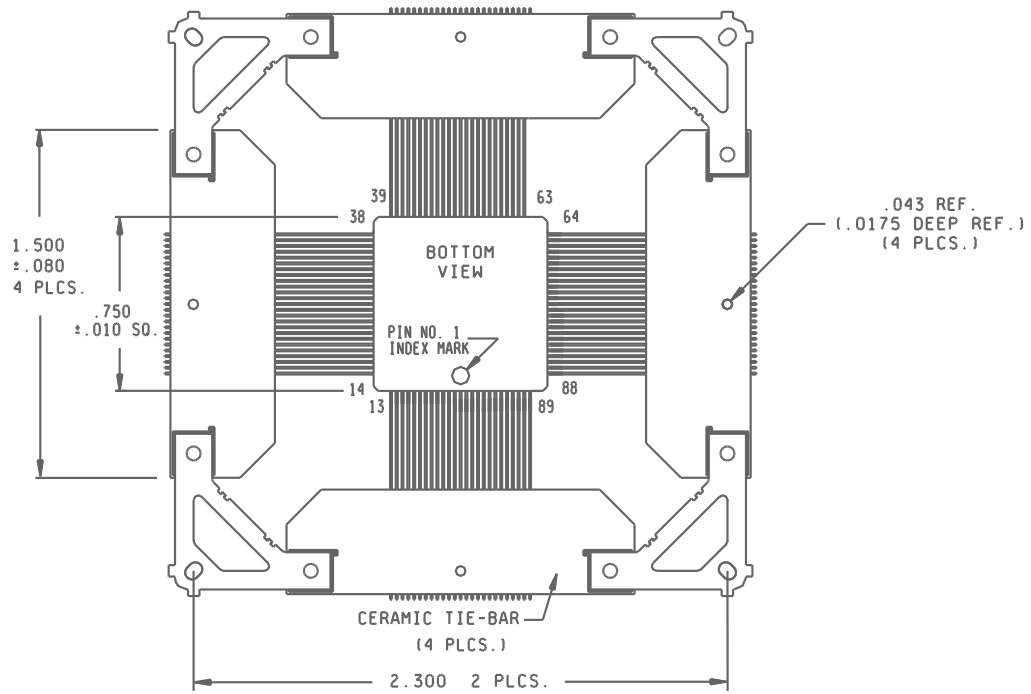
NOTES:

1. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise
2. Dimensions are in inches.
3. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
4. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. May be a notch, dot, or triangle.
5. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline - Continued.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 21

Case M - Continued.

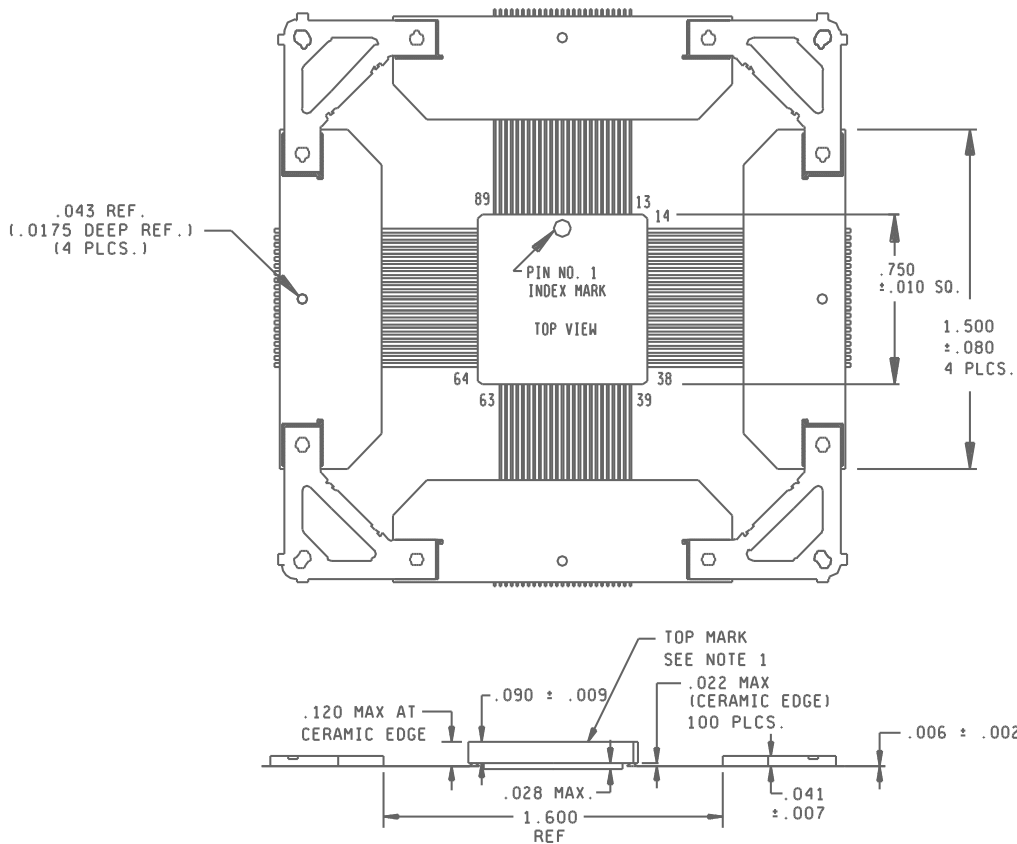


Inches	mm	Inches	mm
.002	0.05	.025	0.64
.006	0.15	.028	0.71
.008	0.20	.030	0.76
.009	0.23	.090	2.29
.010	0.25	.120	3.05
.020	0.51	.600	15.24
.022	0.56	.750	19.05
		2.550	64.77

FIGURE 1. Case outline - Continued.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	SIZE <b>A</b>		<b>5962-89713</b>
		REVISION LEVEL <b>C</b>	SHEET <b>22</b>

Case 9



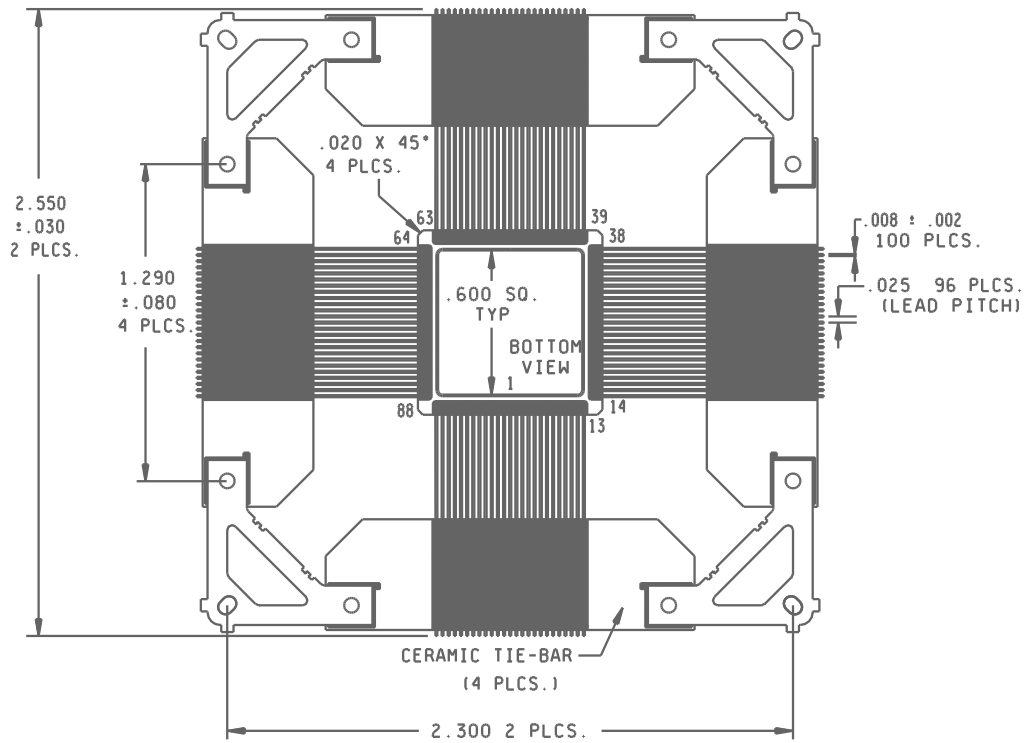
NOTES:

1. Top side mark location, product mark is located on the nonlid side of package; i.e., lid side facing down. When mounted in this position, the pin out is clockwise
2. Dimensions are in inches.
3. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
4. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. May be a notch, dot, or triangle.
5. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline - Continued.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 23

Case 9 - Continued.



Inches	mm	Inches	mm
.002	0.05	.025	0.64
.006	0.15	.028	0.71
.008	0.20	.030	0.76
.009	0.23	.090	2.29
.010	0.25	.120	3.05
.020	0.51	.600	15.24
.022	0.56	.750	19.05
		2.550	64.77

FIGURE 1. Case outline - Continued.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

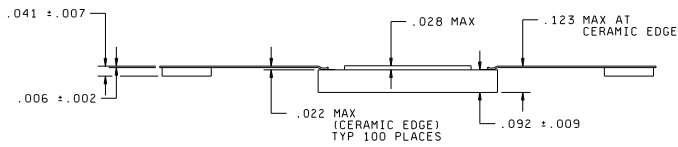
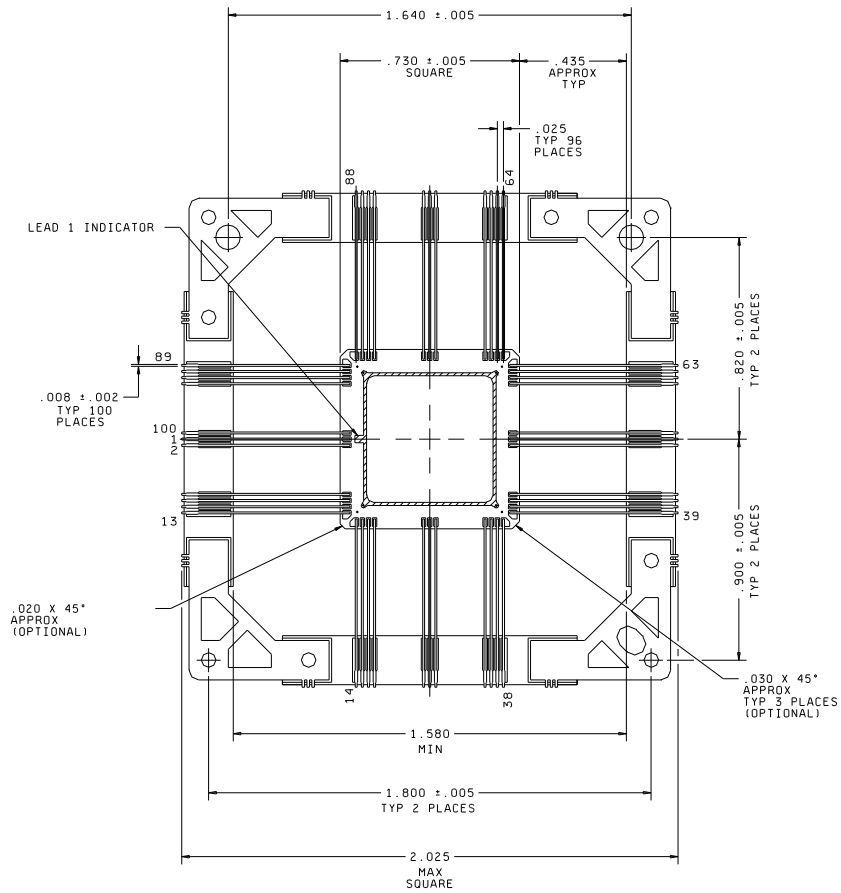
5962-89713

REVISION LEVEL  
C

SHEET  
24



Case 8



	Inches	mm	Inches	mm
.002	.05	.041	1.04	
.005	.13	.092	2.34	
.006	.15	.123	3.12	
.007	.18	.435	11.05	
.008	.20	.730	18.54	
.020	.51	.820	20.83	
.022	.56	.900	22.86	
.025	.64	1.580	40.13	
.028	.71	1.640	41.68	
.030	.76	1.800	45.72	
		2.025	51.44	

FIGURE 1. Case outline - Continued.

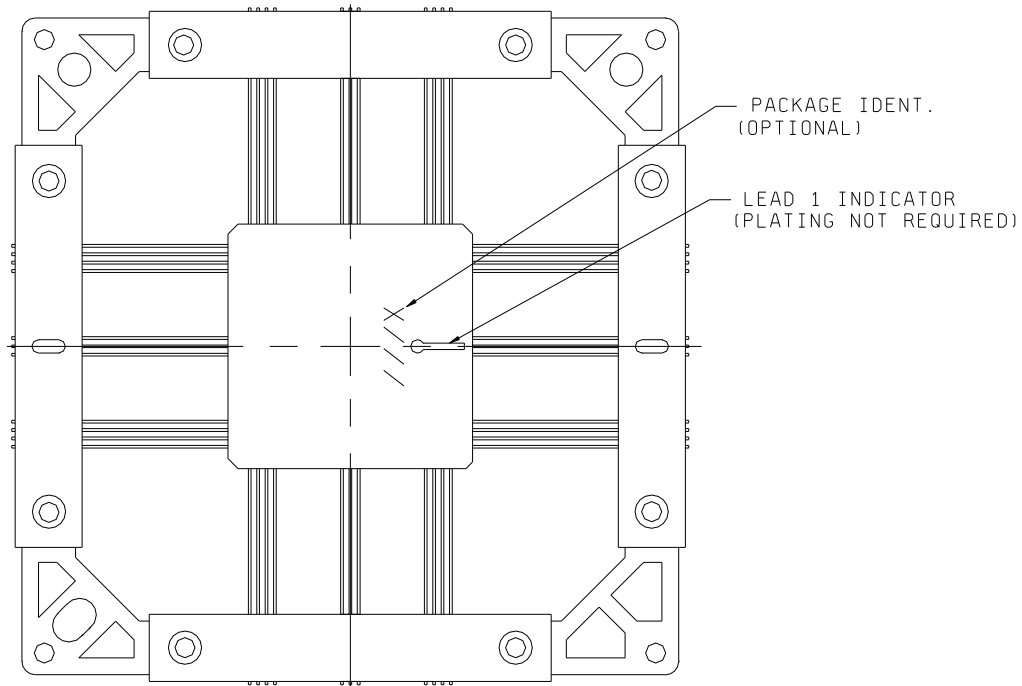
STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-89713

REVISION LEVEL  
C

SHEET  
25



NOTES:

1. Dimensions are in inches.
2. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
3. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. May be a notch, dot, or triangle or other metallized feature.
4. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise.
5. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline - Continued.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	SIZE <b>A</b>		<b>5962-89713</b>
		REVISION LEVEL <b>C</b>	SHEET <b>26</b>

Case outline X and U

Device type	All	Device type	All	Device type	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	A9-I/O	C10	DOUT-I/O	J1	I/O
A2	A8-I/O	C11	RCLK-I/O	J2	M1-RDATA
A3	A11-I/O	D1	I/O	J5	I/O
A4	I/O	D2	I/O	J6	GND
A5	A6-I/O	D10	WRT-D1-I/O	J7	I/O
A6	A13-I/O	D11	I/O	J10	DONE-PG
A7	A14-I/O	E1	I/O	J11	XTL1-I/O-BCLKIN
A8	I/O	E2	I/O	K1	I/O
A9	A3-I/O	E3	I/O	K2	M2-I/O
A10	A2-I/O	E9	I/O	K3	HDC-I/O
A11	CCLK	E10	D2-I/O	K4	I/O
B1	I/O	E11	CS1-I/O	K5	I/O
B2	PWRDWN	F1	I/O	K6	INIT-I/O
B3	A10-I/O	F2	I/O	K7	I/O
B4	I/O	F3	V <sub>CC</sub>	K8	I/O
B5	A12-I/O	F9	V <sub>CC</sub>	K9	I/O
B6	A15-I/O	F10	D5-I/O	K10	MASTER RESET
B7	A4-I/O	F11	D3-I/O	K11	D7-I/O
B8	I/O	G1	I/O	L1	M0-RTRIG
B9	CS2-A1-I/O	G2	I/O	L2	I/O
B10	WS-A0-I/O	G3	I/O	L3	LDC-I/O
B11	DIN-D0-I/O	G9	I/O	L4	I/O
C1	I/O	G10	CS0-I/O	L5	I/O
C2	TCLKIN-I/O	G11	D4-I/O	L6	I/O
C3	INDEX PIN	H1	I/O	L7	I/O
C5	A7-I/O	H2	I/O	L8	I/O
C6	GND	H10	D6-I/O	L9	I/O
C7	A5-I/O	H11	I/O	L10	I/O
				L11	XT2-I/O

FIGURE 2. Terminal connections.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-89713

REVISION LEVEL  
C

SHEET  
27

Case outline Y, T, N, M, 9, and 8

Device type	All	Device type	All	Device type	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	35	I/O	68	D6-I/O
2	A13	36	I/O	69	I/O
3	A6	37	M1-RDATA	70	I/O
4	A12	38	GND	71	I/O
5	A7	39	M0-RTRIG	72	D5-I/O
6	I/O	40	V <sub>CC</sub>	73	CS0
7	I/O	41	M2	74	D4-I/O
8	A11	42	HDC	75	I/O
9	A8	43	I/O	76	V <sub>CC</sub>
10	A10	44	LDC	77	D3-I/O
11	A9	45	I/O	78	CS1
12	V <sub>CC</sub>	46	I/O	79	D2-I/O
13	GND	47	I/O	80	I/O
14	PWRDWN	48	I/O	81	I/O
15	TCLKIN-I/O	49	I/O	82	I/O
16	I/O	50	INIT	83	D1-I/O
17	I/O	51	GND	84	RCLK-RDY/BUSY
18	I/O	52	I/O	85	DIN-D0-I/O
19	I/O	53	I/O	86	DOUT-I/O
20	I/O	54	I/O	87	CCLK
21	I/O	55	I/O	88	V <sub>CC</sub>
22	I/O	56	I/O	89	GND
23	I/O	57	I/O	90	WS-A0
24	I/O	58	I/O	91	CS2-A1
25	I/O	59	I/O	92	I/O
26	V <sub>CC</sub>	60	I/O	93	A2
27	I/O	61	XTL2-I/O	94	A3
28	I/O	62	GND	95	I/O
29	I/O	63	RESET	96	I/O
30	I/O	64	V <sub>CC</sub>	97	A15
31	I/O	65	DONE-PG	98	A4
32	I/O	66	D7-I/O	99	A14
33	I/O	67	BCLKIN-XTL1-I/O	100	A5
34	I/O				

FIGURE 2. Terminal connections - Continued.

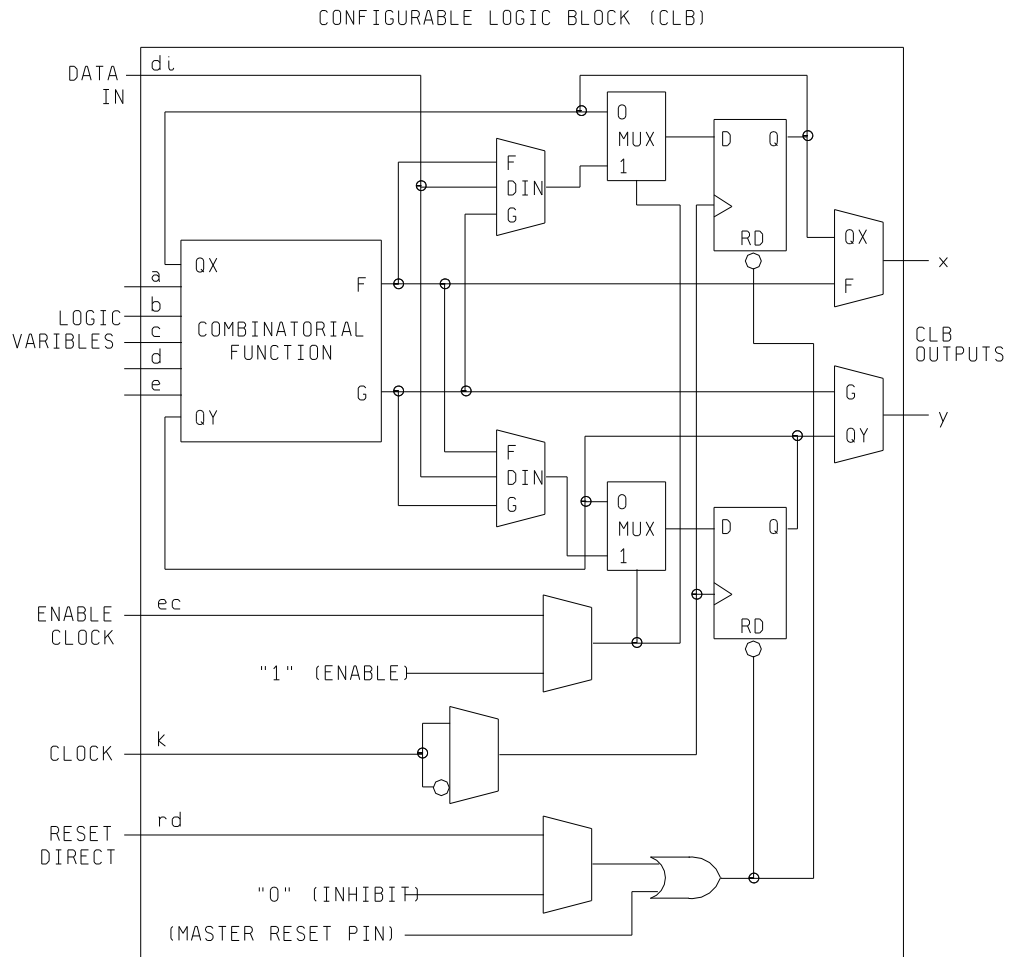
<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	SIZE <b>A</b>		<b>5962-89713</b>
		REVISION LEVEL <b>C</b>	SHEET <b>28</b>

Case outline Z

Device type	All	Device type	All	Device type	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	PWRDN	D3	V <sub>CC</sub>	L13	I/O
A2	N/C	D12	V <sub>CC</sub>	L14	NC
A3	N/C	D13	I/O	M1	I/O
A4	I/O	D14	LDC-I/O	M2	A0-W5-I/O
A5	I/O	E1	A7-I/O	M3	DOOUT-I/O
A6	I/O	E2	I/O	M4	V <sub>CC</sub>
A7	I/O	E3	I/O	M5	D1-I/O
A8	I/O	E12	I/O	M6	D2-I/O
A9	I/O	E13	NC	M7	GND
A10	I/O	E14	I/O	M8	V <sub>CC</sub>
A11	N/C	F1	NC	M9	D5-I/O
A12	N/C	F2	A12-I/O	M10	I/O
A13	N/C	F3	I/O	M11	V <sub>CC</sub>
A14	MO-RT	F12	I/O	M12	D7-I/O
B1	A10-I/O	F13	I/O	M13	XTAL2-I/O
B2	I/O	F14	I/O	M14	I/O
B3	I/O	G1	A6-I/O	N1	A1-CS2-I/O
B4	I/O	G2	A13-I/O	N2	D0-DIN-I/O
B5	I/O	G3	V <sub>CC</sub>	N3	I/O
B6	I/O	G12	V <sub>CC</sub>	N4	RCLK-BUSY/ RDY-I/O
B7	I/O	G13	I/O	N5	I/O
B8	I/O	G14	INIT-I/O	N6	NC
B9	I/O	H1	A14-I/O	N7	D3-I/O
B10	I/O	H2	A5-I/O	N8	D4-I/O
B11	I/O	H3	GND	N9	CS0-I/O
B12	I/O	H12	GND	N10	I/O
B13	M1-RD	H13	I/O	N11	D6-I/O
B14	HDC-I/O	H14	I/O	N12	I/O
C1	I/O	J1	NC	N13	DONE-PG
C2	A9-I/O	J2	A4-I/O	N14	I/O
C3	I/O	J3	I/O	P1	CCLK
C4	GND	J12	I/O	P2	I/O
C5	I/O	J13	I/O	P3	I/O
C6	I/O	J14	I/O	P4	I/O
C7	GND	K1	A15-I/O	P5	NC
C8	V <sub>CC</sub>	K2	I/O	P6	CS1-I/O
C9	I/O	K3	I/O	P7	I/O
C10	I/O	K12	I/O	P8	NC
C11	GND	K13	I/O	P9	NC
C12	I/O	K14	I/O	P10	I/O
C13	M2-I/O	L1	A3-I/O	P11	NC
C14	I/O	L2	A2-I/O	P12	I/O
D1	A11-I/O	L3	GND	P13	XTAL1-I/O
D2	A8-I/O	L12	GND	P14	RESET

FIGURE 2. Terminal connections - Continued.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>	<b>5962-89713</b>
		<b>REVISION LEVEL C</b>

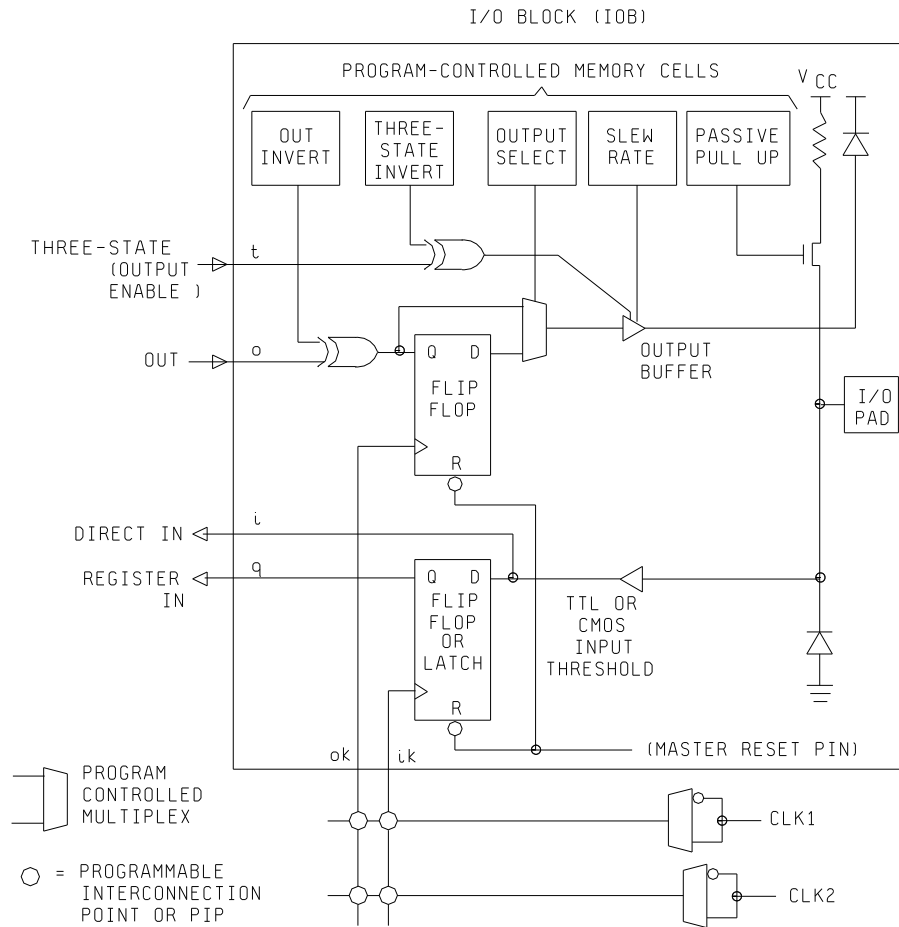


NOTE: Each CLB includes a combinatorial logic section, two flip-flops, and a program memory controlled multiplexer selection of function.

It has: Five logic variable inputs: a, b, c, d, and e  
 A direct data input: di  
 An enable clock: ec  
 A clock (invertible): k  
 An asynchronous reset: rd  
 Two outputs: x and y

FIGURE 3. Logic block diagrams.

<b>STANDARDIZED          MILITARY DRAWING          DEFENSE ELECTRONICS SUPPLY CENTER          DAYTON, OHIO 45444</b>	<b>SIZE          A</b>		<b>5962-89713</b>
		REVISION LEVEL <b>C</b>	SHEET <b>30</b>

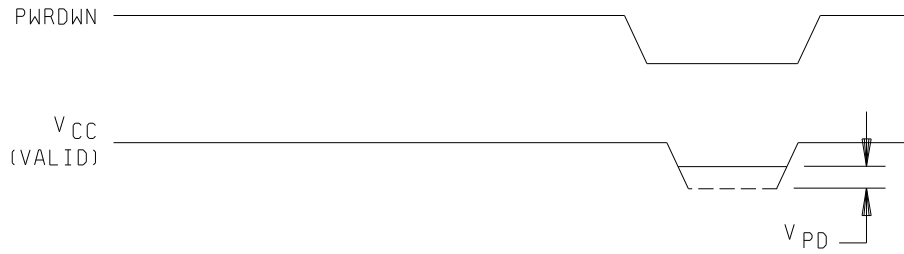


NOTE: The IOB includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active low latch enable (latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

FIGURE 3. Logic block diagrams - Continued.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		<b>REVISION LEVEL C</b>	<b>SHEET 31</b>

GENERAL LOGIC CELL ARRAY (LCA) SWITCHING CHARACTERISTICS



NOTE: All timings except  $t_{TSHZ}$  and  $t_{TSON}$  are measured at 1.5 V levels with 50 pF minimum output load. For input signals, rise and fall times are less than 6.0 ns, with low amplitude = 0 V, and high amplitude = 3.0 V.

FIGURE 4. Timing diagrams and switching characteristics.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 32



CONFIGURABLE LOGIC BLOCK (CLB) SWITCHING CHARACTERISTICS

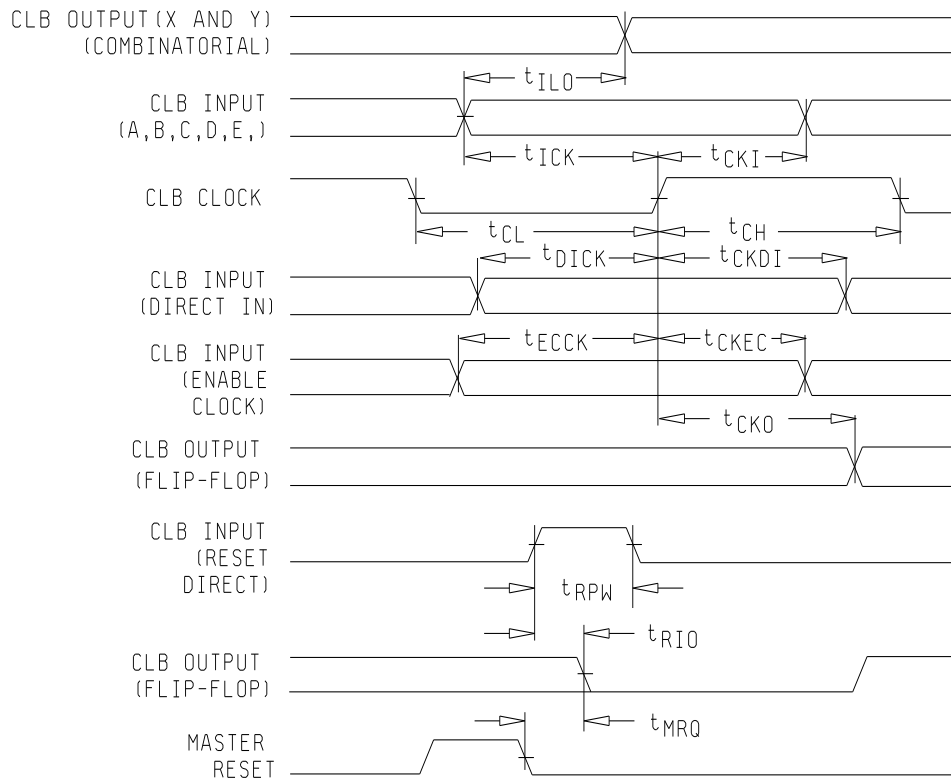


FIGURE 4. Timing diagrams and switching characteristics - Continued.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

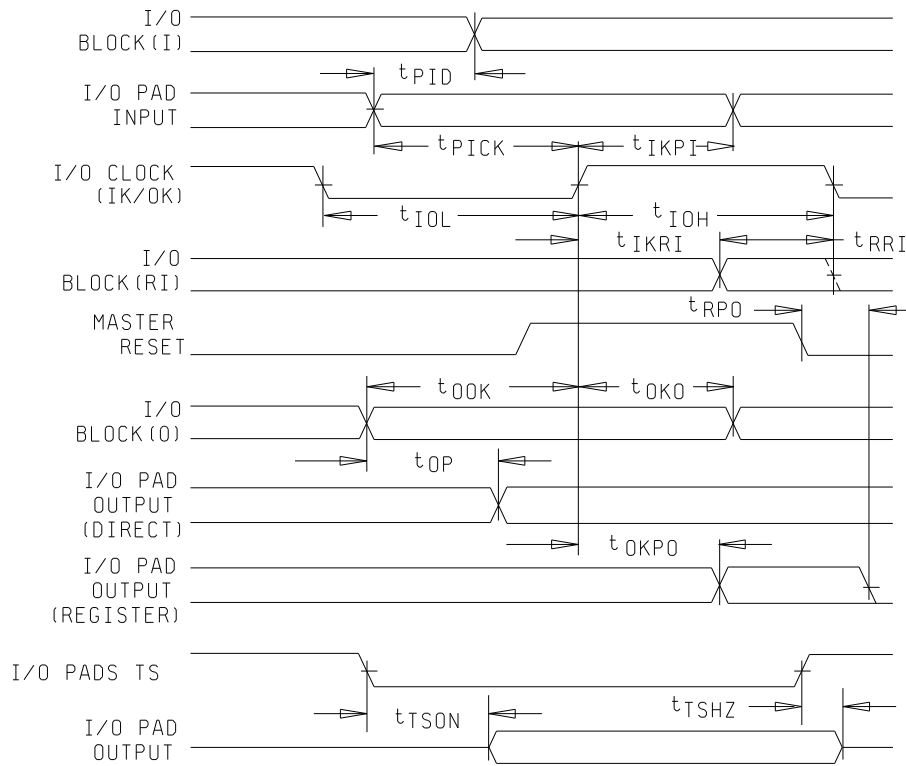
SIZE  
**A**

5962-89713

REVISION LEVEL  
C

SHEET  
33

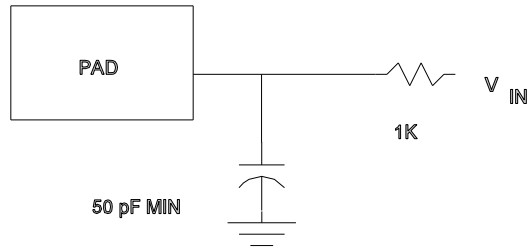
I/O BLOCK (IOB) SWITCHING CHARACTERISTICS



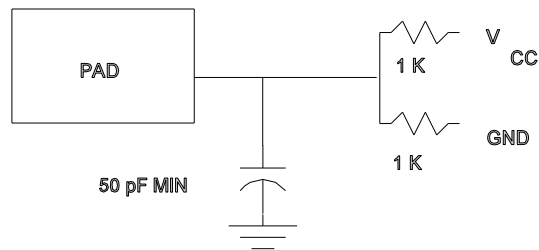
NOTE:  $t_{TSHZ}$  is determined when the output shifts 10 percent (of the output voltage swing) from  $V_{OL}$  level or  $V_{OH}$  level. See figure 5, circuit A herein for circuit used.  $t_{TSON}$  is measured at 0.5  $V_{CC}$  level with  $V_{IN} = 0.0$  V for three-state to active High, and  $V_{IN} = V_{CC}$  for three-state to active low. See figure 5, circuit B herein for circuit used.

FIGURE 4. Timing diagrams and switching characteristics - Continued.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 34



Circuit A



Circuit B

FIGURE 5. Load circuits.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-89713

REVISION LEVEL  
C

SHEET  
35

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)		
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in (method 1015)	Required	Required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Not required	Not required	Not required
5	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
6	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
7	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
8	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
9	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ \* indicates PDA applies to subgroup 1 and 7.

5/ \*\* see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

**STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444**

SIZE  
**A**

**5962-89713**

REVISION LEVEL  
**C**

SHEET  
**36**

TABLE IIB. Delta limits at +25° C.

Parameter 1/	Device types
	All
I <sub>CCO</sub> standby	±300 µA
I <sub>IL</sub> , I <sub>OL</sub>	±2 nA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions.

PWRDWN .....	POWER-DOWN.
MO .....	MODE 0.
RTRIG .....	READ TRIGGER.
M1 .....	MODE 1.
RDATA .....	READ DATA.
M2 .....	MODE 2.
HDC .....	HIGH DURING CONFIGURATION.
LDC .....	LOW DURING CONFIGURATION
RESET .....	RESET
DONE .....	DONE
PG .....	PROGRAM
BCLKIN .....	BCLKIN
XTL1 .....	EXTERNAL CRYSTAL
XTL2 .....	EXTERNAL CRYSTAL
CCLK .....	CONFIGURATION CLOCK
DOUT .....	DATA OUT
DIN .....	DATA IN
CSO .....	CHIP SELECT, WRITE.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 37

6.5 Symbols, definitions, and functional descriptions Continued.

CS1 .....	CHIP SELECT, WRITE.
CS2 .....	CHIP SELECT, WRITE.
WS .....	CHIP SELECT, WRITE.
RCLK .....	READ CLOCK.
RDY/BUSY .....	During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written into it. After configuration is complete, this pin becomes a user programmed I/O pin.
TCLKIN .....	TCLKIN
INIT .....	INIT
D0-D7 .....	DATA
A0-A15 .....	ADDRESS
I/O .....	INPUT/OUTPUT(DEDICATED).
V <sub>CC</sub> .....	+5.0 V SUPPLY VOLTAGE.
GND .....	GROUND

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique part numbers. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique part number. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document</u>
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Additional operating data.

- a. Power on delay is  $2^{14}$  cycles from the non-master mode. This provides 11 to 33 ms of wait time.
- b. Power on delay is  $2^{16}$  cycles for the master mode. This provides 43 to 130 ms of wait time.
- c. Clear is 375 cycles  $\pm$ 25 cycles and may take as long as 250 to 750  $\mu$ s.
- d. During normal power up, V<sub>CC</sub> must rise from 2.0 V to V<sub>CC</sub> minimum in less than 10 ms. If this does not occur, configuration must be delayed by using RESET.

6.8 Sources of supply.

6.8.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.8.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89713</b>
		REVISION LEVEL C	SHEET 38

APPENDIX

10. SCOPE

10.1 Scope. This appendix contains the PIN substitution information to support the one part-one part number system. SMD 5962-89713XXM supersedes SMD 5962-89713. For new designs, after the date of this document the NEW PIN shall be used in lieu of the OLD PIN. For existing designs prior to the date of this document the NEW PIN can be used in lieu of the OLD PIN. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN substitution data shall be as follows.

20. APPLICABLE DOCUMENTS This section is not applicable to this appendix.

30. SUBSTITUTION DATA

<u>New PIN</u>	<u>Old PIN</u>
5962-8971301MXX	5962-8971301XX
5962-8971301MYX	5962-8971301YX
5962-8971301MZX	5962-8971301ZX
5962-8971301MUX	not originally available
5962-8971301MTX	not originally available
5962-8971301MNX	not originally available
5962-8971301MMX	not originally available
5962-8971301M9X	not originally available
5962-8971301M8X	not originally available
5962-8971302MXX	5962-8971302XX
5962-8971302MYX	5962-8971302YX
5962-8971302MZX	5962-8971302ZX
5962-8971302MUX	not originally available
5962-8971302MTX	not originally available
5962-8971302MNX	not originally available
5962-8971302MMX	not originally available
5962-8971302M9X	not originally available
5962-8971302M8X	not originally available
5962-8971303MXX	not originally available
5962-8971303MYX	not originally available
5962-8971303MZX	not originally available
5962-8971303MUX	not originally available
5962-8971303MTX	not originally available
5962-8971303MNX	not originally available
5962-8971303MMX	not originally available
5962-8971303M9X	not originally available
5962-8971303M8X	not originally available
5962-8971304MXX	not originally available
5962-8971304MYX	not originally available
5962-8971304MZX	not originally available
5962-8971304MUX	not originally available
5962-8971304MTX	not originally available
5962-8971304MNX	not originally available
5962-8971304MMX	not originally available
5962-8971304M9X	not originally available
5962-8971304M8X	not originally available

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	SIZE <b>A</b>		<b>5962-89713</b>
		REVISION LEVEL <b>C</b>	SHEET <b>39</b>

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-06-06

Approved sources of supply for SMD 5962-89713 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-8971301MXX	68994	XC3042-50PG84B
5962-8971301MYX	68994	XC3042-50CQ100B
5962-8971301MZX	68994	XC3042-50PG132B
5962-8971301MNX	68994	XC3042-50CQ100B
5962-8971301MMX	68994	XC3042-50CQ100B
5962-8971301M9X	68994	XC3042-50CB100B
5962-8971302MXX	68994	XC3042-70PG84B
5962-8971302MYX	68994	XC3042-70CQ100B
5962-8971302MZX	68994	XC3042-70PG132B
5962-8971302MNX	68994	XC3042-70CQ100B
5962-8971302MMX	68994	XC3042-70CQ100B
5962-8971302M9X	68994	XC3042-70CB100B
5962-8971303MXX	68994	XC3042-100PG84B
5962-8971303MYX	68994	XC3042-100CQ100B
5962-8971303MZX	68994	XC3042-100PG132B
5962-8971303MNX	68994	XC3042-100CQ100B
5962-8971303MMX	68994	XC3042-100CQ100B
5962-8971303M9X	68994	XC3042-100CB100B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number  
68994

Vendor name  
and address  
Xilinx, Incorporated  
2100 Logic Drive  
San Jose, CA 95124

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.



STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-06-06

Approved sources of supply for SMD 5962-89713 are listed below for immediate acquisition only and shall be added to QML-38535 during the next revision. QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of QML-38535.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-8971301QUX	98739	ATT3042-50R84MQ
5962-8971301QTX	<u>2/</u>	ATT3042-50N100MQ
5962-8971301QZX	98739	ATT3042-50R132MQ
5962-8971301Q8X	98739	ATT3042-50N100MQ
5962-8971302QUX	98739	ATT3042-70R84MQ
5962-8971302QTX	<u>2/</u>	ATT3042-70N100MQ
5962-8971302QZX	98739	ATT3042-70R132MQ
5962-8971302Q8X	98739	ATT3042-70N100MQ
5962-8971303QUX	98739	ATT3042-100R84MQ
5962-8971303QTX	<u>2/</u>	ATT3042-100N100MQ
5962-8971303QZX	98739	ATT3042-100R132MQ
5962-8971303Q8X	98739	ATT3042-100N100MQ
5962-8971304QUX	98739	ATT3042-125R84MQ
5962-8971304QTX	<u>2/</u>	ATT3042-125N100MQ
5962-8971304QZX	98739	ATT3042-125R132MQ
5962-8971304Q8X	98739	ATT3042-125N100MQ

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number  
98739

Vendor name  
and address  
AT&T Microelectronics  
555 Union Boulevard  
Allentown, PA 18103

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.