REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added paragraphs 4.4.1e and 4.4.1f, changed Idd value of table IIB from ±1 μA to ±1 mA. ksr	99-04-09	Raymond Monnin

FRONT PAGE HAS BEEN CHANGED

REV																				
SHEET																				
REV	A	A	A	A	A															
SHEET	15	16	17	18	19															

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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CHECKED BY
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APPROVED BY
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DRAWING APPROVAL DATE
96-04-23

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 10,000 GATE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95521**

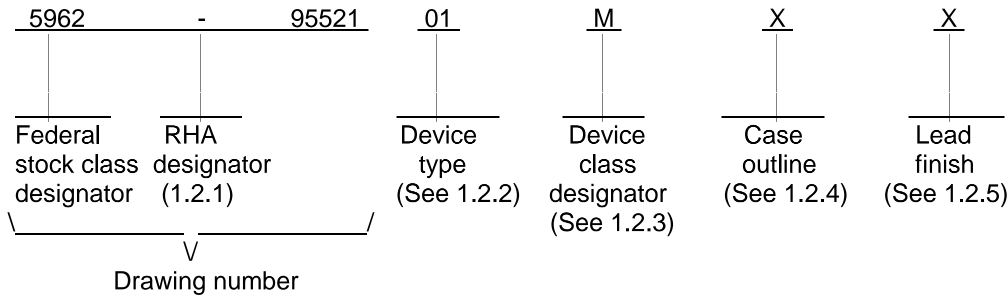
SHEET 1 OF 19

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Toggle Speed
01	14100A	10,000 gate, field programmable array	142.9 ns
02	14100A-1	10,000 gate, field programmable array	121.5 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA11-257C	257 1/	Pin grid array package
Y	See figure 1	256	Quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ 257 = actual number of pins used, not maximum listed in MIL-STD-1835

1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential (V_{DD})	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to V_{DD} +0.5 V dc
Output voltage range	-0.5 V dc to V_{DD} +0.5 V dc
Lead temperature (soldering, 10 seconds)	+300°C
I/O Source/Sink current (I_{IO})	±20 mA.
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X	See MIL-STD-1835
Case outline Y	13°C/W 3/
Junction temperature (T_J)	+150°C 4/
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Case operating temperature Range(T_C)	-55°C to +125°C
Supply voltage relative to ground(V_{DD})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) - - - - - - 6/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ All voltage values in this drawing are with respect to V_{SS}.
6/ Values will be added when they become available.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table.

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or quality conformance inspection group A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be utilized or at least 25 percent of the total number of cells shall be utilized for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device classes M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures on a minimum of ten worst case pins from each device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Programmed device (see 3.2.3.2) - For device class M, subgroups 7, 8A, and 8B tests shall consist of verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012.

f. Unprogrammed devices shall be tested for programmability and dc and ac performance compliance to the requirements of group A, subgroups 1 and 7.

(1) A sample shall be selected from each wafer lot to satisfy programmability requirements. Eight devices shall be submitted to programming (see 3.2.3.1). If any device fails to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(2) These eight devices shall also be submitted to the requirements of the specified tests of group A, subgroups 1 and 7. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3a) Eight devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9 for binning circuit delay only. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3b) If the binning circuit is tested on 100 percent of the products, then the above requirement (3A) is met.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M . Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \leq V_{CC} \leq 5.5\ V$ $-55^oC \leq T_C \leq +125^oC$ 1/ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	Test one output at a time $V_{DD} = 4.5\ V$, $I_{OH} = -4.0\ mA$,	1,2,3	All	3.7		V
Low level output voltage	V_{OL}	Test one output at a time $V_{DD} = 4.5\ V$, $I_{OL} = 6.0\ mA$	1,2,3	All		0.4	V
High level input voltage	V_{IH}		1,2,3	All	2.0		V
Low level input voltage	V_{IL}		1,2,3	All		0.8	V
Input leakage current 2/	I_{IL}	$V_{DD} = 5.5\ V$, $V_{IN} = V_{DD}$ or GND	1,2,3	All	-10	10	μA
Standby supply current	I_{DD}	Outputs unloaded VDD = 5.5 V, $V_{IN} = V_{DD}$ or GND	1,2,3	All		25	mA
Output leakage current	I_{OZ}	$V_{DD} = 5.5\ V$, $V_{IN} = V_{DD}$ or GND	1,2,3	All	-10	10	μA
I/O terminal capacitance	$C_{I/O}$	See 4.4.1c	4	All		20	pF
Functional test	2/		7,8A,8B	All			
Binning circuit delay	t_{PBLH}, t_{PBHL}	See figure 3, $V_{IL} = 0\ V$, $V_{IH} = 3.0\ V$, $V_{DD} = 4.5$, $V_{OUT} = 1.5V$ 3/	9,10,11	01		142.9	ns
				02		121.5	

1/ All tests shall be performed under the worst case condition unless otherwise specified.

2/ Devices are functionally tested using a serial scan test method. Data is shifted into the SDI pin and the DCLK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the PRA, PRB or SDO pins. These tests form a part of the manufacturer's test tape and shall be maintained and available at the approved source(s) of supply upon request by DSCC or the OEM.

3/ Binning circuit delay is defined as the input-to-output delay of a special path called the "binning circuit". The binning circuit consists of one input buffer plus 16 combinatorial logic modules plus one output buffer. The logic modules are distributed along the left side of the device. These modules are configured as non-inverting buffers and are connected through programmed antifuses with typical capacitive loading.

Case Y

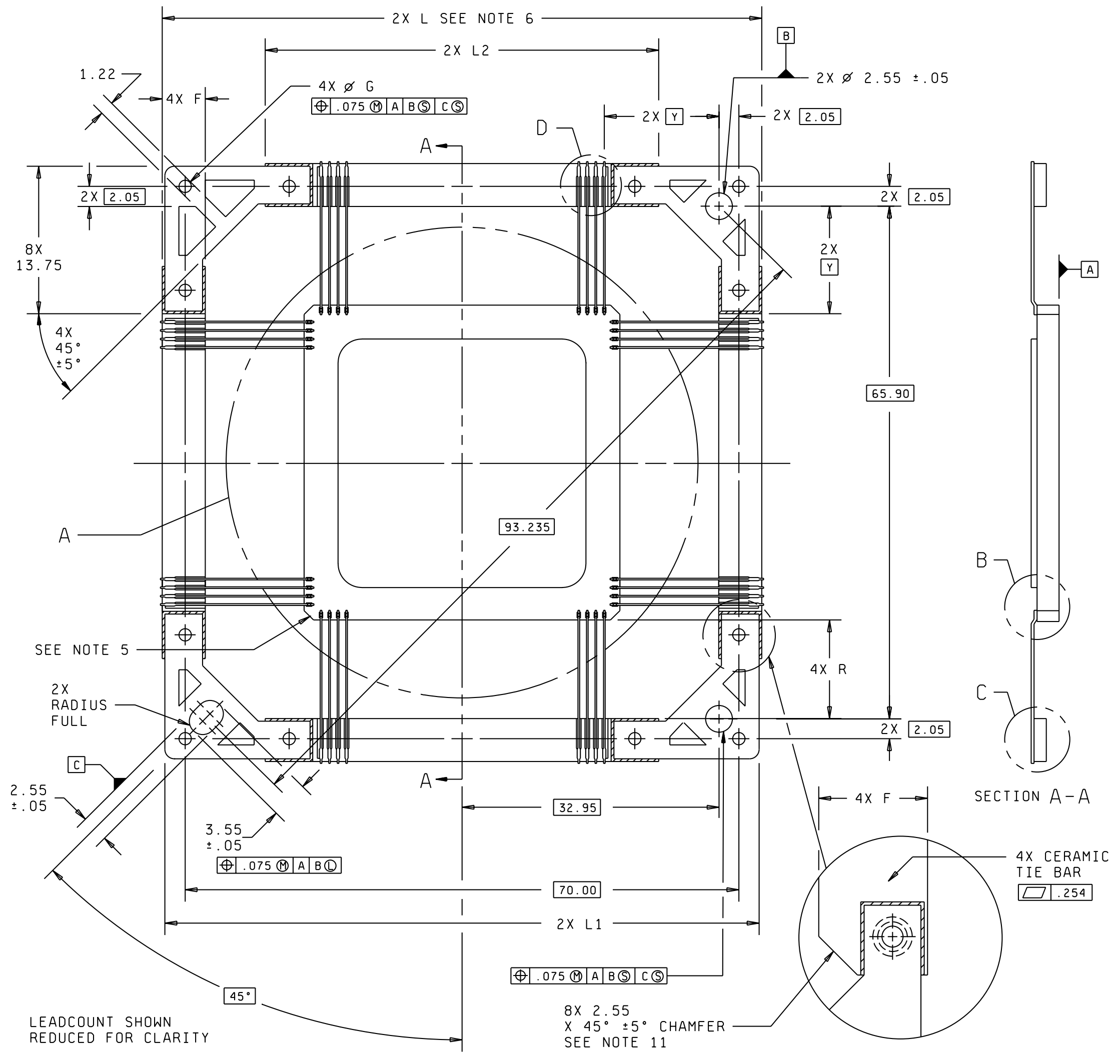


FIGURE 1. Case outline.

Case Y - Continued

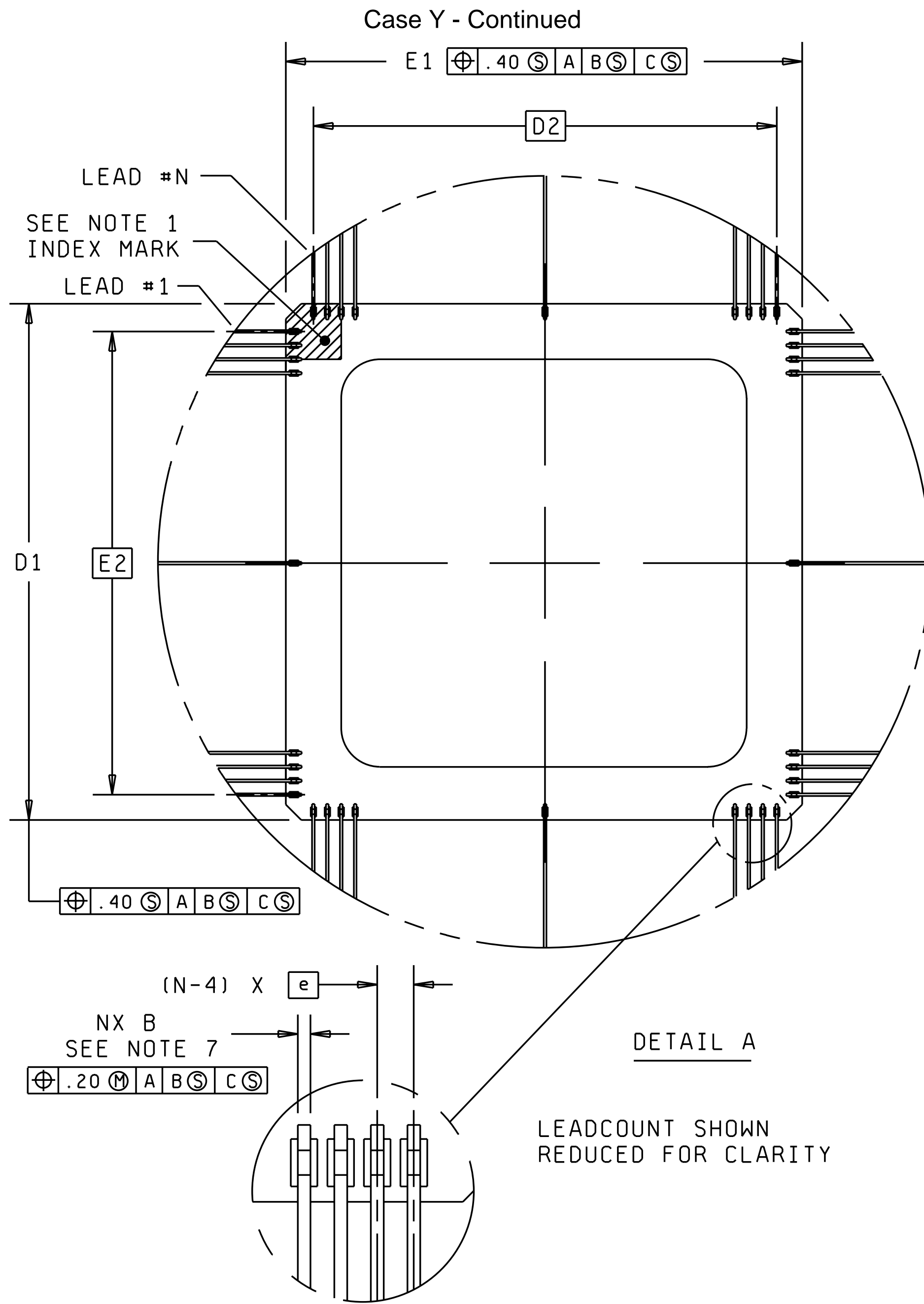


FIGURE 1. Case outline - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316-5000	SIZE A		5962-95521
		REVISION LEVEL A	SHEET 10

Case Y - Continued

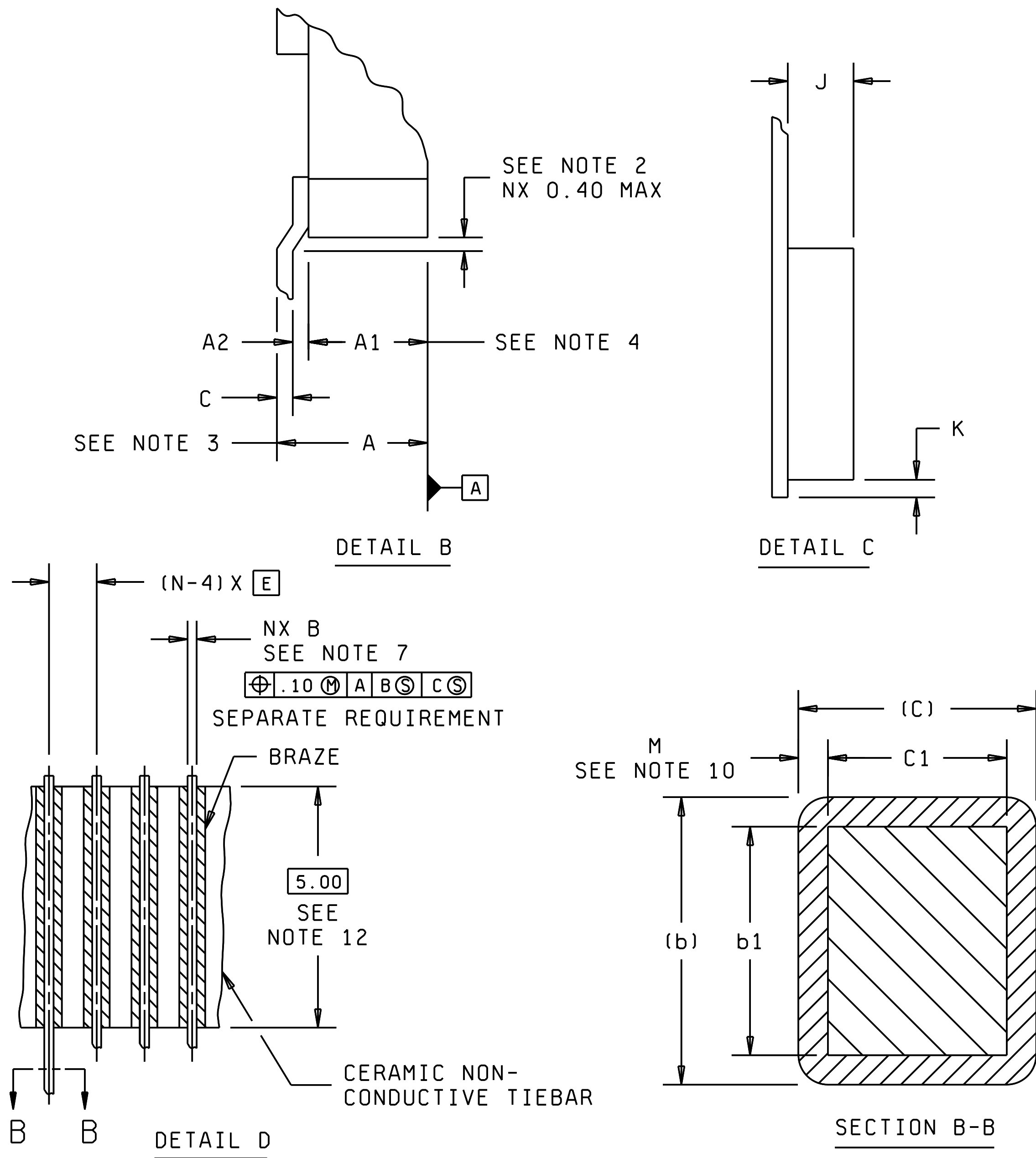


FIGURE 1. Case outline - Continued.

Common Dimensions
Dimensions are in millimeters

SYMBOL	MINIMUM	NOMINAL	MAXIMUM	NOTES
A	2.16	3.55	4.55	3
A1	2.00	3.19	4.00	4
A2	0.05	0.20	0.35	
b	0.19	0.21	0.25	
b1	0.18	0.20	0.22	10
c	0.11	0.16	0.20	
c1	0.10	0.15	0.17	10
e	0.50 BASIC			
G	1.45	1.50	1.55	
J	0.75	0.90	1.05	
K	---	---	0.50	
L	74.85	75.25	76.40	6
L1	74.60	75.00	75.40	
L2	55.60	56.30	57.00	
M	---	---	0.015	
D1 E1	35.64	36.00	36.36	
D2 E2	31.5 BASIC			
F	6.85	7.75	8.65	
N	256			7
ND	64			8
R	10.90	-----	-----	
Y	17.20			
NOTES	9, 13, 14			

NOTES:
1. An index mark shall be located within the shaded area shown.
2. Generic lead attach dogleg depiction. Flat lead configuration is optional.
3. Includes heatsink option. Total thickness includes lead attach dogleg height or lid height, whichever is greater.
4. Includes heatsink option.
5. Edge chamfers are optional, pin #1 may have optional feature (large chamfer or notch) for mechanical orientation purposes.
6. Dimension L, includes maximum lead tip overhang.
7. Dimension N is number of leads.
8. Dimension ND is number of leads per package side or edge.
9. Interpret dimensions and tolerances in accordance with ANSI Y14.5M.
10. Dimension b1 and c1 apply to the base metal only. Dimension M applies to plating thickness.
11. Chamfer tie bar applies to 224 and 256 leadcounts only. Square tie bar applies to 288, 320 and 352 lead counts only.
12. Leadtip position shall be measured in a zone 5mm in length from external edge of ceramic tie bar.
13. All dimensions are in millimeters. Tolerance is ±0.125 mm unless otherwise specified.
14. Features not dimensioned are package supplier's option.

FIGURE 1. Case outline - Continued.

Case outline X

Device type	All	Device type	All	Device type	All	Device type	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	I/O	D2	I/O	J3	I/O	R11	I/O
A2	I/O	D3	I/O	J4	I/O	R13	I/O
A3	I/O	D4	GND	J5	GND	R16	IOPCL,I/O
A4	I/O	D5	I/O	J15	I/O	R17	SDO,I/O
A5	MODE	D6	I/O	J16	FCLK,I/O	R18	I/O
A6	I/O	D7	I/O	J17	PRBB,I/O	R19	I/O
A7	I/O	D8	I/O	J18	I/O	T1	I/O
A8	I/O	D9	I/O	J19	I/O	T2	I/O
A9	I/O	D10	GND	K1	I/O	T3	I/O
A10	I/O	D11	I/O	K2	I/O	T4	GND
A11	I/O	D12	I/O	K3	VCC	T5	IOCLK,I/O
A12	I/O	D13	I/O	K4	GND	T6	I/O
A13	I/O	D14	I/O	K16	GND	T7	I/O
A14	I/O	D15	BINOUT,I/O	K17	VCC	T8	I/O
A15	I/O	D16	GND	K18	I/O	T9	I/O
A16	I/O	D17	I/O	K19	I/O	T10	GND
A17	I/O	D18	I/O	L1	I/O	T11	I/O
A18	I/O	D19	I/O	L2	I/O	T12	I/O
A19	I/O	E1	I/O	L3	I/O	T13	I/O
B1	I/O	E2	I/O	L4	CLKA,I/O	T14	I/O
B2	I/O	E3	I/O	L5	CLKB,I/O	T15	I/O
B3	I/O	E4	DCLK,I/O	L15	GND	T16	GND
B4	SDI/I/O	E7	I/O	L16	I/O	T17	GNDQ
B5	I/O	E9	I/O	L17	I/O	T18	I/O
B6	I/O	E11	GND	L18	I/O	T19	I/O
B7	I/O	E13	I/O	L19	I/O	V1	I/O
B8	I/O	E16	I/O	M1	I/O	V2	I/O
B9	I/O	E17	I/O	M2	I/O	V3	VCC
B10	I/O	E18	I/O	M3	I/O	V4	I/O
B11	I/O	E19	I/O	M4	I/O	V5	I/O
B12	I/O	F1	I/O	M16	I/O	V6	I/O
B13	I/O	F2	I/O	M17	I/O	V7	VPP
B14	I/O	F3	I/O	M18	I/O	V8	I/O
B15	I/O	F4	I/O	M19	I/O	V9	I/O
B16	GNDQ	F16	I/O	N1	I/O	V10	VCC
B17	I/O	F17	I/O	N2	I/O	V11	I/O
B18	I/O	F18	I/O	N3	I/O	V12	I/O
B19	I/O	F19	I/O	N4	I/O	V13	I/O
C1	I/O	G1	I/O	N5	I/O	V14	I/O
C2	I/O	G2	I/O	N15	I/O	V15	I/O
C3	VCC	G3	I/O	N16	I/O	V16	I/O
C4	GNDQ	G4	I/O	N17	I/O	V17	V_{CC}
C5	I/O	G5	I/O	N18	I/O	V18	I/O
C6	I/O	G15	I/O	N19	I/O	V19	I/O
C7	I/O	G16	I/O	P1	I/O	X1	I/O
C8	I/O	G17	I/O	P2	I/O	X2	I/O
C9	I/O	G18	I/O	P3	I/O	X3	I/O
C10	VCC	G19	I/O	P4	I/O	X4	I/O
C11	I/O	H1	I/O	P16	I/O	X5	I/O
C12	I/O	H2	I/O	P17	I/O	X6	I/O
C13	VSV	H3	I/O	P18	I/O	X7	VKS
C14	I/O	H4	I/O	P19	I/O	X8	I/O
C15	BININ	H16	I/O	R1	I/O	X9	I/O
C16	I/O	H17	I/O	R2	I/O	X10	I/O
C17	V_{CC}	H18	I/O	R3	I/O	X11	I/O
C18	I/O	H19	I/O	R4	GNDQ	X12	I/O
C19	I/O	J1	PRBA,I/O	R7	I/O	X13	I/O
D1	I/O	J2	I/O	R9	I/O	X14	VSV

FIGURE 2. Terminal connections.

Case outline X- Continued.

Device type	All
Terminal number	Terminal symbol
X15	I/O
X16	I/O
X17	I/O
X18	I/O
X19	I/O
Y1	I/O
Y2	I/O
Y3	I/O
Y4	I/O
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	I/O
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O

FIGURE 2. Terminal connections - Continued.

Case outline Y

Device type	All	Device type	All	Device type	All	Device type	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GNDQ	57	BININ	113	I/O	169	I/O
2	SDI,I/O	58	BINOUT	114	I/O	170	I/O
3	I/O	59	GNDQ	115	I/O	171	I/O
4	I/O	60	I/O	116	I/O	172	I/O
5	I/O	61	I/O	117	I/O	173	SDO,I/O
6	I/O	62	I/O	118	I/O	174	VPP
7	I/O	63	I/O	119	I/O	175	VKS
8	I/O	64	I/O	120	I/O	176	GNDI
9	I/O	65	I/O	121	I/O	177	I/O
10	I/O	66	I/O	122	I/O	178	I/O
11	MODE	67	I/O	123	I/O	179	I/O
12	I/O	68	I/O	124	I/O	180	I/O
13	I/O	69	I/O	125	I/O	181	I/O
14	I/O	70	I/O	126	SDO,I/O	182	I/O
15	I/O	71	I/O	127	IOPCL,I/O	183	I/O
16	I/O	72	I/O	128	GNDQ	184	I/O
17	I/O	73	I/O	129	I/O	185	I/O
18	I/O	74	I/O	130	I/O	186	I/O
19	I/O	75	I/O	131	I/O	187	I/O
20	I/O	76	I/O	132	I/O	188	IOCLK,I/O
21	I/O	77	I/O	133	I/O	189	GNDQ
22	I/O	78	I/O	134	I/O	190	I/O
23	I/O	79	I/O	135	I/O	191	I/O
24	I/O	80	I/O	136	I/O	192	I/O
25	I/O	81	I/O	137	I/O	193	I/O
26	I/O	82	I/O	138	I/O	194	I/O
27	I/O	83	I/O	139	I/O	195	I/O
28	VCCI	84	I/O	140	I/O	196	I/O
29	GNDA	85	I/O	141	VSV	197	I/O
30	VCCA	86	I/O	142	I/O	198	I/O
31	GNDI	87	I/O	143	I/O	199	I/O
32	I/O	88	I/O	144	I/O	200	I/O
33	I/O	89	I/O	145	I/O	201	I/O
34	I/O	90	PRBB,I/O	146	I/O	202	I/O
35	I/O	91	GNDI	147	I/O	203	I/O
36	I/O	92	VCCI	148	I/O	204	I/O
37	I/O	93	GNDA	149	I/O	205	I/O
38	I/O	94	VCCA	150	I/O	206	I/O
39	I/O	95	I/O	151	I/O	207	I/O
40	I/O	96	FCLK,I/O	152	I/O	208	I/O
41	I/O	97	I/O	153	I/O	209	I/O
42	I/O	98	I/O	154	I/O	210	I/O
43	I/O	99	I/O	155	I/O	211	I/O
44	I/O	100	I/O	156	I/O	212	I/O
45	I/O	101	I/O	157	I/O	213	I/O
46	VSV	102	I/O	158	GNDI	214	I/O
47	I/O	103	I/O	159	VCCA	215	I/O
48	I/O	104	I/O	160	GNDA	216	I/O
49	I/O	105	I/O	161	VCCI	217	I/O
50	I/O	106	I/O	162	I/O	218	I/O
51	I/O	107	I/O	163	I/O	219	CLKA,I/O
52	I/O	108	I/O	164	I/O	220	CLKB,I/O
53	I/O	109	I/O	165	I/O	221	VCCI
54	I/O	110	GNDI	166	I/O	222	GNDA
55	I/O	111	I/O	167	I/O	223	VCCA
56	I/O	112	I/O	168	I/O	224	GNDI

FIGURE 2. Terminal connections - Continued.

Case outline Y- Continued.

Device type	All
Terminal number	Terminal symbol
225	PRBA
226	I/O
227	I/O
228	I/O
229	I/O
230	I/O
231	I/O
232	I/O
233	I/O
234	I/O
235	I/O
236	I/O
237	I/O
238	I/O
239	I/O
240	GNDI
241	I/O
242	I/O
243	I/O
244	I/O
245	I/O
246	I/O
247	I/O
248	I/O
249	I/O
250	I/O
251	I/O
252	I/O
253	I/O
254	I/O
255	I/O
256	DCLK,I/O

FIGURE 2. Terminal connections - Continued.

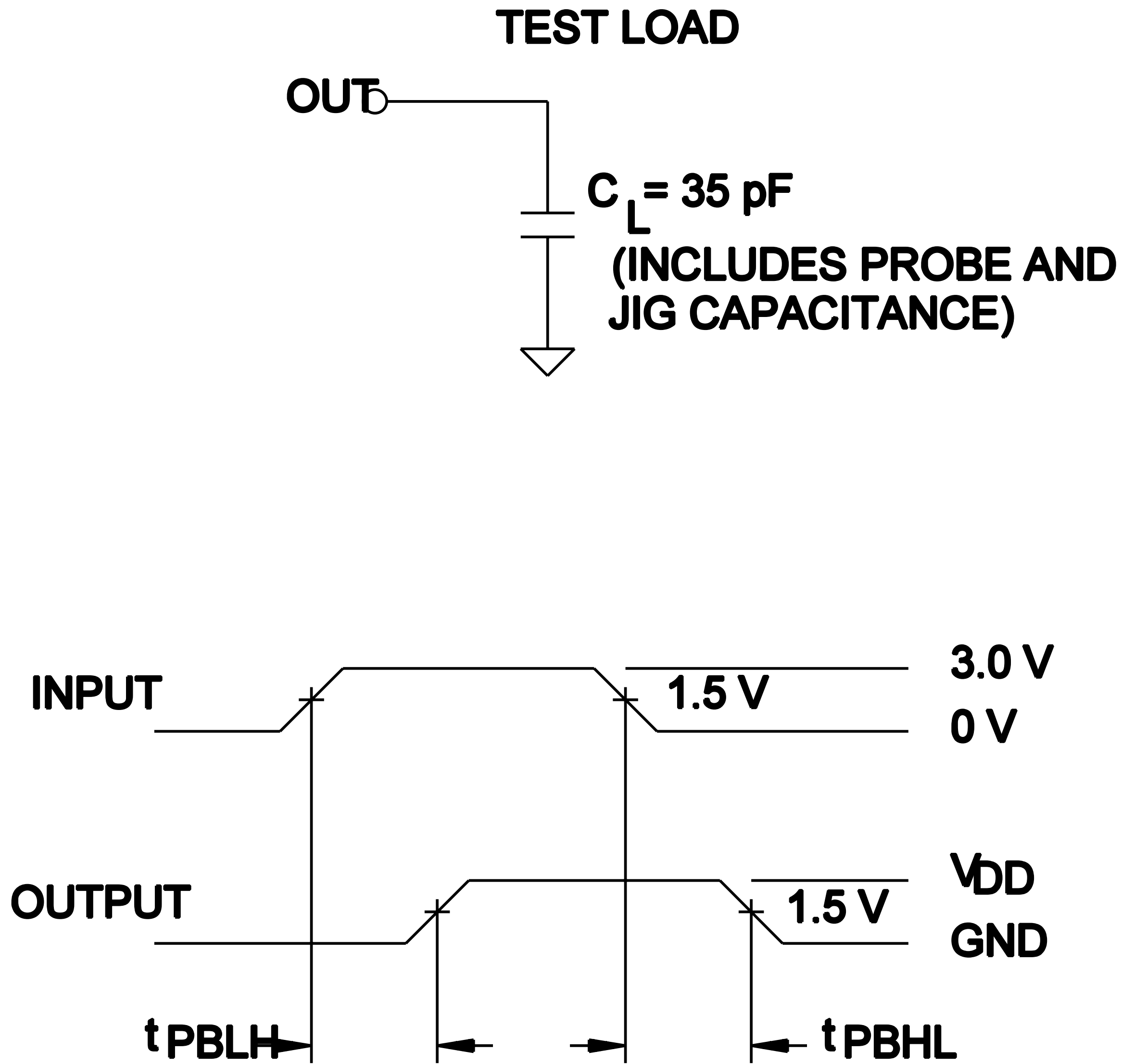


FIGURE 3. Switching test circuit and waveforms.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Not required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
6	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
7	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
8	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
9	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{DD}	±1.0 mA
I_{OZ}	±2 μA
tPBLH, tPBHL	±10 ns

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Sources of supply.

6.5.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.5.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99 - 04 - 09

Approved sources of supply for SMD 5962-95521 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revisions. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9552101MXC	0J4Z0	A14100A PG257B
5962-9552101MYC	0J4Z0	A14100A CQ256B
5962-9552102MXC	0J4Z0	A14100A-1PG257B
5962-9552102MYC	0J4Z0	A14100A-1CQ256B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0J4Z0	Actel Corporation 955 East Arques Ave. Sunnyvale, CA 94086

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.