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RADIATION TEST REPORT

Universal Mini Controller (CPU Card and Power Supplies)

ENGINEERING DIRECTORATE

AVIONICS SYSTEMS DIVISION

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1.0 INTRODUCTION

Candidate elements of the Universal Mini Controller (UMC) were tested at the Indiana University Cyclotron Facility (IUCF) to assess susceptibility of the unit to high-energy ionizing radiation. There are no current implementations of the UMC; however, the system is being looked at for use in the TransHab and Mars projects, as well as Orbiter upgrades. The test was conducted on November 12, 1999, with all test results provided in this report.

The members of the test team were:

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2.0 TEST OBJECTIVES

The objectives of the radiation testing were to obtain data to make preliminary estimates of ionizing radiation induced functional interrupt rates and other error rates that can be expected on orbit.

3.0 BACKGROUND

A definition of the test philosophy and the radiation environment model used is presented in this section.

3.1 Radiation Test Philosophy Hardware elements must be able to operate in the environment for the duration of their missions. The two major elements of the ionizing radiation environment are the deposition of energy from Total Ionizing Dose (TID) and the Single Event Effects (SEE) produced by high energy particles like protons and atomically heavier ions. The TID experienced by any hardware element is a function of its location on the vehicle. Shielding values are available for various locations within the spacecraft. The SEE's experienced on orbit are not substantially mitigated by shielding because of the high energy of the particles producing the effects.

Radiation testing for SEE's with high energy protons is designed to establish the susceptibility of a given test article to trapped protons in the South Atlantic Anomaly (SAA) and heavy ions due to Galactic and Solar Cosmic Rays. A SEE can be detected as:

- **Single Event Upset (SEU)** – an event like a bit flip resulting in a data error only.

- **Functional Interrupt (FI)** – an event requiring a software reboot or a power cycle.
- **Single Event Latchup (SEL)** – an event where the device has an abnormal conduction path established by the ionizing radiation and as indicated by a primary power supply current change. Power must be recycled to regain control and/or to save the device from destruction.
- **Single Event Burnout (SEB)** – an event where the device has an abnormal conduction path established by the ionizing radiation and is destroyed almost immediately.

The occurrence of a SEE is a single sample observed from a random process. The more samples (in this case SEE's detected) observed, the better the estimate of the Mean Time Between Failures (MTBF) for that specific type of SEE. The goals of this testing are to establish estimates of the MTBF's for each type of SEE detected for a given test article or electronic component.

The probability of an SEE occurring within a test article is related to the number of particles per square centimeter (called fluence) allowed to impinge on the device. The general criterion used in testing with protons is to expose each beam position or test article to a fluence of 10 billion (1E10) protons/cm2.

Even though the SEE susceptibilities measured during testing were only from proton testing, the MTBF's cited in this report are the composite MTBF's due to the nominal proton (primarily SAA trapped protons) and the nominal heavy ion (Galactic Cosmic Rays) environments. The procedures for deriving the MTBF's were determined using the software tool PRODUCT [10]. The proton SEE MTBF's from proton test results were determined using the Bendel A method and are described in [6]. The heavy ion SEE MTBF from proton test results was calculated as described in [5] and [7], using the formula:

MTBF = 6 years/Number of SEE's in 1E10 protons/cm2

3.2 Radiation Environment Definition For typical orbits for the space shuttle or the space station considered here (51.6 - 57 degree inclination, 270 nmi altitude), the nominal ionizing radiation environment consists of Galactic Cosmic Rays and trapped protons and electrons. The Galactic Cosmic Ray flux was modeled with a solar modulation algorithm [1], [2] whose accuracy has been demonstrated over four solar cycles. The trapped proton and electron radiation spectrum was generated using the AP8 model with solar minimum conditions (1964 epoch, 1965 International Geomagnetic Reference Field (IGRF)) [3]. Orbit average environments were determined for solar minimum conditions with 0.1" thick spherical aluminum shielding for quiet conditions and no earth shadow. Transport and geomagnetic shielding models can be found in [4]. The trapped electron spectrum was only used for TID calculations. These environments are consistent with those defined in [8] and [9].

4.0 GENERAL DISCUSSION

All testing was done with a proton beam energy of 190 Million-electron Volts (MeV). The normal beam diameter of approximately 6 cm was passed through various copper vignettes to adjust the size of the final beam allowed to radiate the test article. The beam positions and required vignettes were pre-planned and documented (see Appendix A) in the expected order of execution.

4.1 Test Hardware
These candidate elements for the UMC system were tested:
1. UMC Central Processor Unit (CPU)
2. UMC Power Supply #1 (PS1)
3. UMC Power Supply #2 (PS2)

On November 12, 1999, all of the above components were tested (see section 5 for test summary).

4.2 Test Setup Configuration The test configuration consisted of the UMC CPU, PS1, and PS2 in the test chamber ("cave"). Individual power supplies (5v, 3.3v, and 2.5v) provided the required power for the CPU. The CPU was connected to the test room via RS232 for communication purposes. Current was monitored in the test room using the Radiation Watchdog (RAD DOG) hardware/software system using a laptop. A laptop was also used to monitor the CPU test execution. Built in hardware/software error flags on the CPU card were monitored for radiation induced errors. The CPU card also enabled error checking and correction (ECC) for the 32 Megabytes of onboard DRAM. ECC is capable of detecting and correcting single bit errors, and detecting double bit errors. For this test, the CPU was configured to only count double bit errors, single bit errors were not reported. (NOTE: Memory scrubbing was not performed, allowing single-bit errors to propagate into multi-bit errors and, therefore, be detected.

For the Power Supply tests, the current was monitored using digital multi-meters. A camera was set up in the "cave" to view the multi-meters and the data was monitored in the test room via closed-circuit television.

5.0 SUMMARY OF TESTING

The following sections discuss the results of testing each UMC element. Included in the discussion are the MTBF's noted for the elements that reacted to the beam. The MTBF's reported are the errors expected from both protons and heavy ions.

5.1 UMC Central Processing Unit Figure 1 shows the UMC CPU in the test configuration.

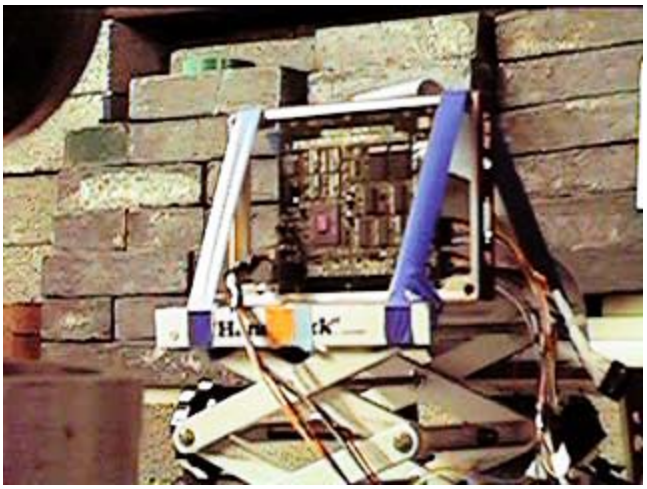

Figure 1. UMC Central Processing Unit

Seven positions were tested on this unit. Two of the seven positions reacted to the beam.

Position	Number of Failures	Failure Type	Recovery Method	MTBF (years)
3	3	SEU (3)	Manual Restart*	1.63
7**	8	FI (8)**	Auto Recovery	0.61
Total UMC CPU Failures		**SEU (3)** **FI (8)**	**Manual Restart*** **Auto Recovery**	**1.63** **0.61**

* The failures for this position were multi-bit errors and were detected using the EDAC software. These errors were DRAM errors. "Manual Restart" indicated in the table above represents the lack of memory scrubbing. Memory scrubbing was not performed, allowing single-bit errors to propagate into multi-bit errors and, therefore, detected. The software was restarted and testing continued. Flight software will institute memory scrubbing.

** Position 7 was the same as Position 6 with one exception. Position 6 had the internal cache of the PowerPC 603e microprocessor turned off, while Position 7 had the internal cache turned on. All errors were observed with the cache on and were recovered with an auto reset by the Watchdog Timer (WDT).

5.2 UMC Power Supply #1 Figure 2 shows the UMC PS1 in the test configuration. Three positions were tested on this unit with no failures noted.

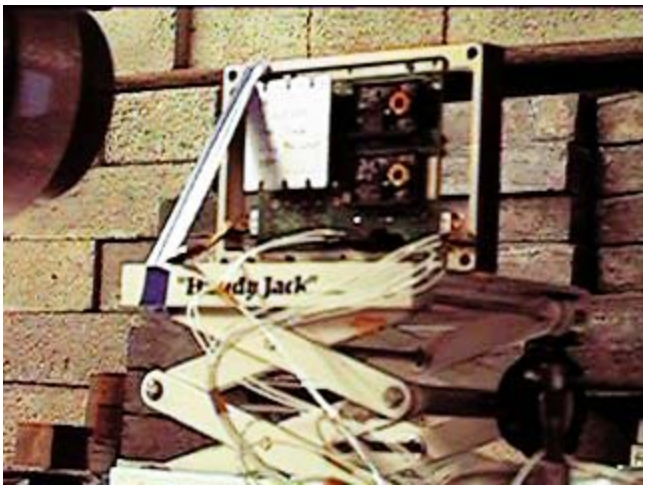

Figure 2. UMC Power Supply #1

5.3 UMC Power Supply #2 Figure 3 shows the UMC PS2 in the test configuration. Four positions were tested for this unit with no failures noted.

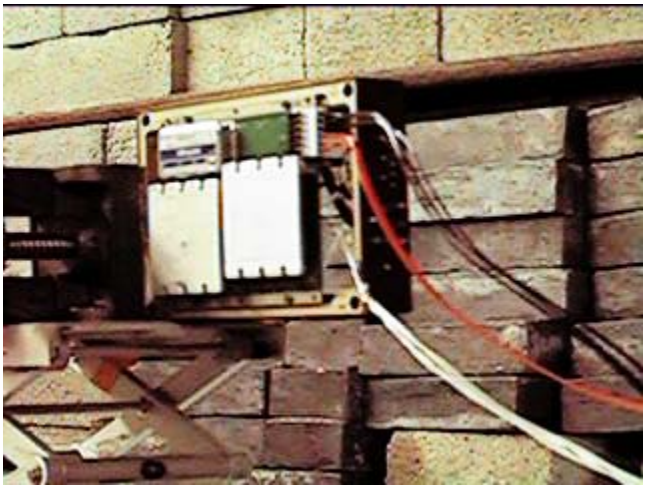

Figure 3. UMC Power Supply #2

6.0 CONCLUSIONS

Each position of all units tested received a minimum fluence of 1E10 protons/cm2, which is equivalent to a TID of 600 Rads(Si). No degradation in performance due to the TID was noted. All test articles were operational at the end of the test.

- The MTBF for the UMC CPU Single Event Upset is 1.63 years and the MTBF for the UMC CPU Functional Interrupt recovering automatically is 0.61 years.

- Neither UMC PS1 nor UMC PS2 had any failures from radiation testing.

The total MTBF for both the UMC Single Event Upset and Functional Interrupt recovering automatically is 1.63 years with the internal cache disabled, and 0.44 years with the internal cache enabled.

REFERENCES

1. Badhwar, G. D. and P.M. O'Neill, "Galactic Cosmic Radiation Model and Its Applications", Advances in Space Research, Vol. 17, No. 2, 1996.

2. Badhwar, G. D. and P.M. O'Neill, "Time Lag of Twenty Two Year Solar Modulation", Proceedings of the International Cosmic Ray Conference, SH 6.21, Calgary, July 19-30, 1993.

3. Sawyer, D. M. and J.I. Vette, "AP8 Trapped proton Environment for Solar Minimum and Solar Maximum", National Space Science Data Center Report NSSDC/WDC-A-R&S 76-06, NASA-GSFC TMS-72605, December, 1976.

4. Adams Jr., J. H., "Cosmic Ray Effects on Microelectronics, Part IV", Naval Research Laboratory Memorandum Report 5901, December 31, 1986.

5. O'Neill, P. M., G. D. Badhwar, and W. X. Culpepper, "Internuclear Cascade - Evaporation Model for LET Spectra of 200 MeV Protons Used for Parts Testing," IEEE Trans. Nuclear Science, (Dec. 1998).

6. Bendel, W. L. and E. L. Petersen, "Proton Upsets in Orbit," IEEE Trans. Nuclear Science, NS-30, 4481, (Dec. 1983).

7. E. L. Petersen, "The SEU Figure of Merit and Proton Upset Rate Calculations," IEEE Trans. Nuclear Science, (Dec. 1998).

8. Space Station Ionizing Radiation Design Environment, Rev C: International Space Station Alpha, NASA SSP30512 Revision C, (June 1994).

9. NSTS 07700, Volume X, Book 1 and Book 2.

10. O'Neill, P. M., "Computer Code for Calculating On Orbit Single Event Effect (SEE) Rates Based on Proton Test Data," NASA Internal Memo EA44-98-28, (Nov. 1998).

APPENDIX A: UMC PARTS LIST & BEAM POSITION

Circuit Board	Part Number	Part Description	Manufacturer	LDC	Loc.	Beam Pos.	Also Affected by beam #	Note
CPU Board	Fox 143	Crystal	FOX		X1			
CPU Board	CDC2586PAH	Clock Driver	TI		U1	1		1” x 1.5”
CPU Board	PI74ALVCH16501A	Transceiver, 18-Bit Bus	Perfcom		U11	1		1” x 1.5”
CPU Board	PI74ALVCH16501A	Transceiver, 18-Bit Bus	Perfcom		U12	1		1” x 1.5”
CPU Board	PI74ALVCH16501A	Transceiver, 18-Bit Bus	Perfcom		U13	1		1” x 1.5”
CPU Board	PI74ALVCH16501A	Transceiver, 18-Bit Bus	Perfcom		U14	1		1” x 1.5”
CPU Board	CDC9643DW		TI		U2	2		1” x 1.5”
CPU Board	PC16550DVEF	UART	NSC		U7	2		1” x 1.5”
CPU Board	MT4LC4M16R6TG-5	DRAM, x16	Micron		U15	3		1” x 2.5”
CPU Board	MT4LC4M16R6TG-5	DRAM, x16	Micron		U16	3		1” x 2.5”
CPU Board	MT4LC4M16R6TG-5	DRAM, x16	Micron		U38	3		1” x 2.5”
CPU Board	MT4LC4M16R6TG-5	DRAM, x16	Micron		U39	3		1” x 2.5”
CPU Board					U20	4		1” x 2.5”
CPU Board	Am29LV160BB-90EC	EEPROM, x8/x16 Flash	AMD		U27	4		1” x 2.5”
CPU Board	Am29LV160BB-90EC	EEPROM, x8/x16 Flash	AMD		U29	4		1” x 2.5”
CPU Board	NC7S08P5	Single 2-input AND Gate	Fairchild		U34	4		1” x 2.5”
CPU Board	Am29LV160BB-90EC	EEPROM, x8/x16 Flash	AMD		U36	4		1” x 2.5”
CPU Board	Am29LV160BB-90EC	EEPROM, x8/x16 Flash	AMD		U37	4		1” x 2.5”
CPU Board	74F139	2-to-4 line Demultiplexer	Philips		U5	4		1” x 2.5”

CPU Board	N74F138D	3-to-8-Line Demultiplexer	Philips		U21	5		1.875” x 1.875”
CPU Board	NC7S04P5	Single Inverter	Fairchild		U28	5		1.875” x 1.875”
CPU Board	XPC603PFE166LE	Microprocessor	MOT		U3	5		1.875” x 1.875”
CPU Board	XPC106ARX66CG	Microprocessor	MOT		U4	5		1.875” x 1.875”
CPU Board	74LVTH162244DL	Quad 4-Bit Buffer/Driver	TI		U10	6		1.875” x 1.875”
CPU Board	74LCX543MTC	Single 8-Bit Bus Transceiver	Fairchild		U17	6		1.875” x 1.875”
CPU Board	HM51W16405LTS-6	DRAM, x4	Hitachi		U18	6		1.875” x 1.875”
CPU Board	W83C553F	Peripheral Controller	Windbond		U22	6		1.875” x 1.875”
CPU Board	NC7S08P5	Single 2-input AND Gate	Fairchild		U30	6		1.875” x 1.875”
CPU Board	NC7S08P5	Single 2-input AND Gate	Fairchild		U31	6		1.875” x 1.875”
CPU Board	NC7S08P5	Single 2-input AND Gate	Fairchild		U32	6		1.875” x 1.875”
CPU Board	NC7S08P5	Single 2-input AND Gate	Fairchild		U33	6		1.875” x 1.875”
CPU Board	HM51W16405LTS-6	DRAM, x4	Hitachi		U40	6		1.875” x 1.875”
CPU Board	NC7S04P5	Single Inverter	Fairchild		U41	6		1.875” x 1.875”
CPU Board	NC7SZ32P5	Single 2-Input OR Gate	Fairchild		U43	6		1.875” x 1.875”
CPU Board	NC7SZ02P5	Single 2-input NOR Gate	Fairchild		U44	6		1.875” x 1.875”
CPU Board	NC7S04P5	Single Inverter	Fairchild		U45	6		1.875” x 1.875”
CPU Board	NC7SZ126P5	Single Buffer	Fairchild		U46	6		1.875” x 1.875”
CPU Board	MAX813LCUA	Power Supply Supervisor	Maxim		U6	6		1.875” x 1.875”
CPU Board	MAX3221EAE	Transceiver	Maxim		U8	6		1.875” x 1.875”
CPU Board	74LVTH162244DL	Quad 4-Bit Buffer/Driver	TI		U9	6		1.875” x 1.875”

Power Supply 1	MI-A22-MU	DC/DC Converter	Vicor		U1	1		1.875” x 1.875”
Power Supply 1	MI-21-MY	DC/DC Converter	Vicor		U2	2		1.875” x 1.875”
Power Supply 1	MHD2812S/01	DC/DC Converter	Interpoint		U3	3		1.875” x 1.875”
Power Supply 2	MI-J20-MY	DC/DC Converter	Vicor		U1	1		1.875” x 1.875”
Power Supply 2	MC7S204		Fairchild		U6	1		1.875” x 1.875”
Power Supply 2	MC7S204		Fairchild		U7	1		1.875” x 1.875”
Power Supply 2	SMHF2805S/00	DC/DC Converter	Interpoint		U3	2		1.875” x 1.875”
Power Supply 2	PT6501G	Voltage Regulator	Power Trend		U4	3		1.875” x 1.875”
Power Supply 2	PT6503G	Voltage Regulator	Power Trend		U5	4		1.875” x 1.875”